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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R § 1.53(b))

Attorney Docket No.	68135469-205220 (P04329 P01)
First Inventor	Peyman Hojabri
Title	MULTIPLEXED VIDEO SIGNAL INERFACE SIGNAL, SYSTEM AND METHOD
Express Mail Label No.	EL563098702US

jc926 U.S. PTO 09/698719 10/27/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Commissioner for Patents
Box Patent Application
Washington DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing.)
2. ☒ Specification [Total Pages 49]
(preferred arrangement as set forth below)
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed Sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. ☒ Drawing(s) *(35 U.S.C 113)* [Total Sheets 34]
4. ☒ Oath or Declaration [Total Pages 2]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 C.F.R. §1.63(d))
   (for continuation/division with Box 16 completed)
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b)
5. ☐ Microfiche Computer Program *(Appendix)*
6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement PTO-1449
    ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Report Postcard (MPEP 503)
13. ☐ Small Entity Statement
    ☐ Statement filed in prior application, status still proper
14. ☐ Certified Copy of Priority Document(s)
15. ☐ Other:

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☐ Continuation ☐ Divisional ☒ Continuation-in-part (CIP) of prior application No.: 09/602,175, filed: 06/22/00.

Prior application information: Examiner: Unknown Group Art Unit: 2731

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Date: October 27, 2000

EXPRESS MAIL NO.: EL563098702US

FEE TRANSMITTAL
For FY 2001

Patent Fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	($1738)

Complete if Known	
Application Number	NEW
Filing Date	HEREWITH
First Named Inventor	Peyman Hojabri
Examiner Name	Not Yet Assigned
Group Art Unit	Not Yet Assigned
Attorney Document No.	68135469-205220 (P04329 P01)

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

50-0974
BAKER & MCKENZIE

Deposit Account Number & Deposit Account Name

☒ Charge any additional fees required under 37 CFR §§ 1.16 and 1.17
☐ Applicant claims small entity status.

2. ☒ **Payment Enclosed:**
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

LARGE ENTITY Fee Code	Fee ($)	SMALL ENTITY Fee Code	Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility	710
106	320	206	160	Design	
107	490	207	245	Plant	
108	710	208	355	Reissue	
114	150	214	75	Provisional	
				SUBTOTAL (1)	$710

2. EXTRA CLAIM FEES

		Extra Claims	Fee from below	Fee Paid
Total Claims	26 - 20 **	= 6	x 18	= $ 108
Independent	14 - 3	=11	x 80	= $ 880
Multiple Dep.			*	= $ *

*** or number previously paid, if greater; for Reissues, see below:*

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description
103	18	203	9	Claim in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue ind. claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) $988

FEE CALCULATION (continued)

3. Additional Fees

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee	
139	130	139	130	Non-English specification	
147	2520	139	2520	Filing a request for re-examination	
112	920*	112	920*	Req. publ. of SIR prior to Ex. Action	
113	1840*	113	1840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within 1st mo.	
116	390	216	195	Extension for reply within 2nd mo.	
117	890	217	445	Extension for reply within 3rd mo.	
118	1390	218	695	Extension for reply within 4th mo.	
128	1890	228	945	Extension for reply with 5th mo.	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1510	138	1510	Pet to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1240	241	620	Petition to revive - unintentional	
142	1240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petition related to provisional apps.	
126	240	126	240	Submission of IDS Statement	
581	40	581	40	Recording each patent assignment per property (x no. of properties)	40
146	710	246	355	Filing a submission after final rej.	
149	710	249	355	For each add'l. invention to be examined (37 C.F.R. § 1.129(b))	
Other fee (specify):					

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** $40

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Rev. 10/01/00

MULTIPLEXED VIDEO SIGNAL INTERFACE SIGNAL, SYSTEM AND METHOD

RELATED APPLICATIONS

This application is a Continuation-In-Part of U.S. Patent Application No. 09/602,175, filed June 22, 2000, and entitled "Multiplexed Video Signal Interface Signal, System and Method." This application also claims the benefit of U.S. Provisional Application No. 60/153,013, filed September 9, 1999. This application is also related to U.S. Patent Application No. 09/271,027, filed March 17, 1999, and entitled "Multiplexed Video Interface System," and to U.S. Patent Application No. 09/348,533, filed July 7, 1999, and entitled "Digitally Controlled Signal Magnitude Control Circuit." The disclosure of each of the foregoing applications is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit architecture for generating component video signals for driving a display device such as a cathode ray tube (CRT), and in particular, to a technique for generating such component signals using signal multiplexing.

2. Description of the Related Art

A computer system essentially comprises a system unit housing a microprocessor, computer memory, and various other support logic, as well as various input/output (I/O) devices which are connected to the system unit and enable a user to intelligently interact with the system unit. Examples of various types of input devices include a keyboard, a mouse, a trackball, and a pen computer, as well as others. The primary output device in a computer system include a video display monitor (video monitor).

Video monitors, such as for use with digital computers, include a cathode ray tube (CRT), and driver circuitry including a video amplifier. The CRT includes three primary color cathode ray guns which are manipulated to converge on a screen that produces the color image. The three guns produce converged scanning rasters having red, green and blue fields which combine to produce white light. The typical scanning raster is a left to

right horizontal and top to bottom vertical scan operated in accordance with the Video Electronics Standards Association (VESA) requirements.

A conventional monitor amplifier circuit 100 for displaying screen control states of a monitor is illustrated in Fig. 1. In general, low level color video signals blue b, red r, and green g from a video source (not shown), such as a personal computer (PC) are provided to respective video preamplifiers 101a, 101b and 101c. These preamplifiers in turn provide the respective video signals blue b, red r, and green g, via buffer amplifiers BUFF11, BUFF12, BUFF13, to video output driver stages 103a, 103b, 103c which supply high level amplified color video signals B, R and G to respective cathode intensity control electrodes of a CRT (not shown). As can be seen, in Fig. 1, each video signal blue b, red r, and green g is applied to a respective amplifier circuit AMP11-AMP13, each of which includes four main components: a video preamplifier 101a-101c, a bias/brightness circuit 105a-105c, a video amplifier 103a-103c, and a clamp amplifier 107a-107c. Since the monitor amplifier circuits AMP11-AMP13 are identical in structure and operation, only the circuit operation of amplifier circuit AMP12 for the red video signal r will be discussed by referring to Fig. 2.

As can be seen in Fig. 2, the four main components of monitor amplifier circuit AMP12 are numbered 1-4, number 1 being bias/brightness circuit 105b, number 2 being video preamplifier 101b, number 3 being clamp amplifier 107b, and number 4 being video amplifier 103b.

Operation of this red video channel r is as follows. Terminal 10 constitutes the red video signal input r which originates from an external source, such as a PC. Capacitor CAP12 couples the red video signal r to the noninverting input of video preamplifier 101b.

At this point, the amplification of red video signal r is controlled by a single-throw switch SW12 and a video clamp pulse VC. In any video signal, the clamp pulses are developed just following the synchronization pulses and make it possible to restore the voltage reference level of a video signal, in this case red video signal r. This clamp pulse VC is located in the "back porch" of the composite red video signal r and is employed to operate switch SW12. When clamp pulse VC is high, switch SW12 is closed. Thus, each time the CRT scans a horizontal line, capacitor CAP12 will be charged to black level reference voltage VREF, which is the potential reference level of the black region of an image. This level corresponding to the black color in an image makes it possible to restore the potential reference level of the red video signal r, this level having disappeared

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on account of the presence of the input capacitor CAP12.

On the other hand, when video clamp pulse VC is low, switch SW12 opens and red video signal r is applied directly to video preamplifier 101b, which is shown in Fig. 2 as a unity gain amplifier. Thus, red video signal r is passed through video preamplifier 101b.

At this point, the amplification of red video signal r is controlled by double-throw switch SW14 and signal 11. Signal 11 represents a horizontal blanking pulse that is derived from the display scanning circuits in a manner well known in video display monitors. This signal 11 is employed to operate a double-throw switch SW14 which switches the input IN12 to output buffer BUFF12, between the output of video preamplifier 101b and circuit ground. When signal 11 is high, input IN12 couples to video preamplifier 101b, the output of which is inversely amplified by video amplifier 103b to a voltage level suitable for driving a CRT and then applied to cathode electrodes of the CRT. On the other hand, when signal 11 is low, input IN12 is at circuit ground and the CRT is blanked by driving the output of the video amplifier 103b to a high level.

During operation of this amplifier circuit AMP12, output coupling capacitor CAP 22 changes the DC level at the CRT cathode. Thus, a bias clamp circuit 105b is used to restore the DC level at the CRT cathode through a series diode D11. Bias clamp circuit 105b outputs a bias clamp DC voltage which, in a typical video monitor, is usually factory set. This bias clamp voltage reinstates the charge on output capacitor CAP22 only during the blanking period. The voltage is preset, typically, in the range of 100-140 volts to compensate for differences in CRT cathode bias levels, required by each cathode in the CRT to set the black level. In addition, an adjustable voltage component of typically +/- 10 volts may be added to this bias level to accomplish the 'brightness' feature, such that the black level can be manually adjusted by an external source. Thus, for example, increased image brightness results when the bias clamp voltage is reduced. This results in a less positive DC bias potential at the red cathode and a related increase in image brightness.

Although the conventional monitor amplifier system 100 amplifies and conditions video signals to drive the CRT, there are several disadvantages to the circuit configuration. Referring again to Fig. 1, it can be seen that this architecture involves a significant number of interconnections. Such a low level of integration has several disadvantages. First, the circuit architecture requires a large printed circuit board (PCB), yielding higher design costs due to shielding for the radio frequency (RF) interface. Second, the conventional circuit architecture has inferior high frequency performance due to long

interconnection traces between the components and due to electromagnetic interference (EMI) stemming from long signal lines and large signal swings across the video interface between each preamplifier 101a-101c and corresponding video amplifier 103a-103c. Third, the high number of interconnections require higher pin count packages which are undesirably large and expensive. Finally, the complexity of the system 100 due to the low level of integration results in longer design time.

Referring to Figure 3, a conventional video display circuit 200a shown in more detail includes, as three of its primary integrated circuits, a pre-amplifier 202, an on-screen display (OSD) generator and pulse width modulation (PWM) circuit 204, and a CRT driver 206, interconnected substantially as shown. The pre-amplifier 202 clamps and amplifies the component blue 201b, green 201g and red 201r video signals, while providing gain and contrast control as well as the ability to introduce OSD characters. The OSD and PWM circuit 204 receives the horizontal 201h and vertical 201v blanking signals and a set 201i of control signals (based upon the well-known I2C signal standard) and in accordance therewith generates OSD character information signals 205o and gain and contrast control signals 205pa for the pre-amplifier 202.

The PWM control signals 205pa, 205pb, 205pc are filtered by a PWM filter circuit 208 to provide corresponding filtered control signals 205paf, 205pbf, 205pcf.

The horizontal 201h and vertical 201v blanking signals are also combined in a buffer circuit 216 to produce a composite blanking signal 217 for the pre-amplifier 202.

The amplified and clamped component video signals 203b, 203g, 203r are further amplified by the CRT driver 206 to produce the higher voltage component video signals 207b, 207g, 207r needed to drive the CRT. These signals, 207b, 207g, 207r are themselves clamped using DC clamp signals 211b, 211g, 211r provided by a high voltage DC clamp circuit 210 which receives its control signals 205pbf via the PWM filter circuit 208.

The vertical blanking signal 201v is further shaped with a pulse shaper circuit 212. The resulting shaped signal 213 is clamped and buffered in a circuit 214 in accordance with a filtered control signal 205pcf to produce the drive signal 215 for the grid of the CRT.

As noted above, this circuit 200a has a number of disadvantages, including numerous interconnections between the integrated circuits. Accordingly, with reference to Figure 4, another conventional system 200b has been used in which the output signals 227b, 227g,

227r from the CRT driver 226 are DC-coupled to the CRT. Further simplification is achieved by incorporating separate I2C interfaces for the control signals 201i within the pre-amplifier 222 and OSD generator 224 circuits. This system avoids the need for both the PWM filters 208 and the high voltage DC clamp circuit 210.

However, this circuit 200b has its own disadvantages. One disadvantage is limited adjustment range for bias clamp adjustment, brightness adjustment, and horizontal and vertical blanking. Additionally, the higher bias voltage required for the CRT driver 226 introduces some new problems. For example, the DC-coupled CRT driver 226 has a limited signal range and dissipates significantly higher power due to the high power supply voltage. Additionally, saturation and storage effects are worse due to the higher voltage processing required for such a high voltage circuit, thereby requiring more DC voltage headroom. Plus, since higher voltage devices are necessarily larger, they have more capacitance, thereby resulting in lower speed, more power and higher cost.

Referring to Figure 5, another problem involves the need for multiple DC power supplies for biasing the CRT 270 correctly. Several electrodes within the CRT 270 require precise voltages and signals in order to ensure that the video information is displayed correctly on the screen.

A typical CRT monitor assembly 260 has component video signal amplifiers 262r, 262b, 262g, a vertical blanking amplifier 264, adjustable bias clamp circuits 266r, 266b, 266g for the component video signals, a high voltage bias supply circuit 268 and a CRT 270, all interconnected substantially as shown. The component video signals 261r, 261b, 261g are amplified by their respective amplifiers 262r, 262b, 262g. The resulting amplified video signals 263r, 263b, 263g are then AC-coupled to respective cathodes of the CRT 270. The adjustable bias clamp circuits 266r, 266b, 266g set the DC voltage level of the signals 267r, 267b, 267g driving the cathodes at the appropriate level so that a black video signal results in the appropriate cathode-to-grid potential to create a black image on the screen of the CRT 270.

Each adjustable bias clamp circuit 266r, 266b, 266g is powered via a common voltage supply 268, typically at a value of approximately 120 volts. This typically requires a power supply winding rectification and smoothing capacitor within the power supply 268 and, of course, connections from the power supply to the individual clamp circuits 266r, 266b, 266g. Such connections can create an antenna that produces radio frequency interference (RFI) due to the very high frequencies within the video amplifier circuits. To

minimize this RFI, any power supply wiring connected to the video amplifiers generally require additional RFI decoupling circuits 272 at the circuit card interface, as shown.

An additional requirement in video amplifiers is a negative-going video pulse 261v to blank the screen during the vertical scan retrace interval. Typically, a pulse is taken from the vertical deflection stage, processed to form a bilevel pulse and used to drive an amplifier 264 which creates a rectangular pulse of approximately 30-40 volts peak-to-peak. This pulse is usually AC-coupled into the grid one of the CRT to ensure that the cathode-to-grid one potential is driven beyond cutoff (i.e., no light output) during the retrace interval. This blanking amplifier typically includes one or more transistors configured as a low power amplifier.

The vertical blanking amplifier 264 and the 120 volt power supply 268 add cost and components to the design of a CRT monitor. Accordingly, it would be desirable to somehow eliminate the needs for these functions, thereby reducing circuit components and costs.

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SUMMARY OF THE INVENTION

A multiplexed video signal interface in accordance with the present invention provides a multiplexed component video signal which includes component video signals with OSD data and user-controllable contrast and video gain, along with the ability to individually control such signal components. This advantageously minimizes the complexity of the necessary signal interfaces and allows for greater integration of circuit functions, thereby significantly reducing circuit complexity, size and costs. Also provided is a signal peaking circuit in the form of a variable high pass filter that enhances the magnitudes of the higher frequency signal components of the component video signals and OSD data, thereby providing for sharper edges on the displayed images.

In accordance with one embodiment of the present invention, a signal multiplexor for controlling and multiplexing video image and on-screen-display (OSD) signals includes control circuits and combining circuits. A first control circuit, following reception of a first reference signal, a contrast control signal and a clamped video signal, provides a first controlled signal with a contrast-controlled video component. A first signal combining circuit, coupled to the first control circuit, in response to a first combining control signal, receives and selectively combines an OSD signal and the first controlled signal to thereby

provide a first combination signal with the contrast-controlled video component and an OSD component. A second control circuit, coupled to the first signal combining circuit, following reception of the first combination signal, the first reference signal and a gain control signal provides a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component. A second signal combining circuit, coupled to the second control circuit, in response to a second combining control signal, receives and selectively combines the second controlled signal and a second reference signal to thereby provide a multiplexed signal with the contrast-controlled and gain-controlled video component, the gain-controlled OSD component and a reference signal component.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information includes: a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information and conveyed via a signal medium includes: a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information for conveyance via a signal medium includes: a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a method of controlling and multiplexing video image and on-screen-display (OSD) signals includes the steps of:

receiving a first reference signal, a contrast control signal and a clamped video signal and in response thereto generating a first controlled signal with a contrast-controlled video component;

receiving a first combining control signal and in response thereto receiving and selectively combining an OSD signal and the first controlled signal and thereby generating a first combination signal with the contrast-controlled video component and an OSD component;

receiving the first combination signal, the first reference signal and a gain control signal and in response thereto generating a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component; and

receiving a second combining control signal and in response thereto receiving and selectively combining the second controlled signal and a second reference signal and thereby generating a multiplexed signal with the contrast-controlled and gain-controlled video component, the gain-controlled OSD component and a reference signal component.

In accordance with another embodiment of the present invention, a multiplexed signal recorded on a recording medium and containing controlled video image and on-screen-display (OSD) information includes: a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a recording medium having recorded thereon a multiplexed signal containing controlled video image and on-screen-display (OSD) information for controlling a display of the video image has been prepared by the steps of:

recording a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

recording a gain-controlled OSD component representing a portion of an OSD image for display as another portion of the composite display image on the display device; and

recording a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a signal multiplexor for controlling and multiplexing video image and on-screen-display (OSD) signals includes control circuits, signal combining circuits and a variable filter circuit. A first control circuit, following reception of a first reference signal, a contrast control signal and a clamped video signal, provides a first controlled signal with a contrast-controlled video component. A first signal combining circuit, coupled to the first control circuit, in response to a first combining control signal, receives and selectively combines an OSD signal and the first controlled signal to thereby provide a first combination signal with the contrast-controlled video component and an OSD component. A second control circuit, coupled to the first signal combining circuit, following reception of the first combination signal, the first reference signal and a gain control signal, provides a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component. A second signal combining circuit, coupled to the second control circuit, in response to a second combining control signal, receives and selectively combines the second controlled signal and a second reference signal to thereby provide a multiplexed signal with the contrast-controlled and gain-controlled video component, the gain-controlled OSD component and a reference signal component. The variable filter circuit, coupled to the second signal combining circuit, in response to a plurality of filter control signals, selectively filters the multiplexed signal to thereby provide a filtered multiplexed signal with the contrast-controlled and gain-controlled video component and the gain-controlled OSD component having enhanced high frequency signal magnitudes.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information includes: a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a

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reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information and conveyed via a signal medium includes: a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a multiplexed signal containing controlled video image and on-screen-display (OSD) information for conveyance via a signal medium includes: a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a method of controlling and multiplexing video image and on-screen-display (OSD) signals includes the steps of:

receiving a first reference signal, a contrast control signal and a clamped video signal and in response thereto generating a first controlled signal with a contrast-controlled video component;

receiving a first combining control signal and in response thereto receiving and selectively combining an OSD signal and the first controlled signal and thereby generating a first combination signal with the contrast-controlled video component and an OSD component;

receiving the first combination signal, the first reference signal and a gain control signal and in response thereto generating a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component;

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receiving a second combining control signal and in response thereto receiving and selectively combining the second controlled signal and a second reference signal and thereby generating a multiplexed signal with the contrast-controlled and gain-controlled video component, the gain-controlled OSD component and a reference signal component; and

receiving a plurality of filter control signals and in response thereto selectively filtering the multiplexed signal and thereby generating a filtered multiplexed signal with the contrast-controlled and gain-controlled video component and the gain-controlled OSD component having enhanced high frequency signal magnitudes.

In accordance with another embodiment of the present invention, a multiplexed signal recorded on a recording medium and containing controlled video image and on-screen-display (OSD) information includes: a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device; a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of the composite display image on the display device; and a reference component representing a blanked portion of the composite display image on the display device.

In accordance with another embodiment of the present invention, a recording medium having recorded thereon a multiplexed signal containing controlled video image and on-screen-display (OSD) information for controlling a display of the video image has been prepared by the steps of:

recording a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

recording a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of the composite display image on the display device; and

recording a reference component representing a blanked portion of the composite display image on the display device.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a functional block diagram of a conventional CRT driver system.

Figure 2 is a functional block diagram of a single channel of the system of Figure 1.

Figure 3 is a functional block diagram of another conventional CRT driver system.

Figure 4 is a functional block diagram of still another conventional CRT driver system.

Figure 5 is a functional block diagram of a CRT monitor assembly.

Figure 6 is a functional block diagram of a multiplexed video signal interface system in accordance with one embodiment of the present invention.

Figure 7 is a functional block diagram of one channel of the system of Figure 6.

Figure 8 illustrates signal diagrams for a multiplexed video signal interface system in accordance with another embodiment of the present invention.

Figure 9 is a functional block diagram of an alternative embodiment of one channel of the system of Figure 6.

Figure 10 is a signal diagram of a multiplexed video signal in accordance with another embodiment of the present invention.

Figure 11 is a graph of an input-to-output signal transfer characteristic for the demultiplexing portion of a multiplexed video signal interface system in accordance with another embodiment of the present invention.

Figure 12 is a functional block diagram of a multiplexed video signal interface system in accordance with another embodiment of the present invention.

Figure 13 is a functional block diagram for the video signal path for one channel of the circuit of Figure 12.

Figure 14 is a signal diagram for representative signals of the system of Figure 12.

Figure 15 is a signal diagram illustrating contrast control provided by the system of Figure 12.

Figure 16 is a signal diagram illustrating gain control provided by the system of Figure 12.

Figure 17 is a signal diagram illustrating bias control provided by the system of Figure 12.

Figure 18 is a signal diagram of a multiplexed video signal provided by the system of Figure 12.

Figure 19 is a functional block diagram of one technique used for clamping the incoming component video signal in the system of Figure 12.

Figure 20 is a schematic diagram of the demultiplexing portion of the system of Figure 12.

Figure 21 is a graph of the input-to-output transfer characteristic for the circuit of Figure 20.

Figure 22 is a graph illustrating the high voltage boost supply and grid blanking pulse output upon system start-up.

Figure 23 is a schematic diagram of a combined high voltage boost and blanking amplifier circuit in accordance with another embodiment of the present invention.

Figure 24 is a signal diagram illustrating the start-up waveforms for the circuit of Figure 23.

Figure 25 is a functional block diagram of a combined high voltage boost and vertical blanking amplifier in accordance with another embodiment of the present invention.

Figure 26 is a signal diagram illustrating the start-up waveforms for the circuit of Figure 25.

Figure 27 is a schematic diagram of one embodiment of an actual circuit implementation of the circuit of Figure 25.

Figure 28 is a functional block diagram of an analog signal system using a digitally controlled signal magnitude control circuit in accordance with one embodiment of the present invention.

Figure 29 is a circuit schematic diagram representing the operation of the digitally controlled signal magnitude control circuit of Figure 28.

Figure 30 is a signal diagram representing the signal magnitude control provided by the circuit of Figure 28.

Figure 31 is a functional block diagram of an analog signal system using a digitally controlled signal magnitude control circuit in accordance with another embodiment of the present invention.

Figure 32 is a graph representing the operation of the digitally controlled signal magnitude control circuit of Figure 31 when used to control the attenuation profile of a variable DC signal.

Figure 33 is a signal diagram representing the signal magnitude control provided by the circuit of Figure 31.

Figure 34 is a circuit schematic diagram of an example embodiment of the digitally controlled signal magnitude control circuits of Figures 28 and 31.

Figure 35 is a circuit schematic diagram of another example embodiment of the digitally controlled signal magnitude control circuits of Figures 28 and 31.

Figure 36 is a schematic diagram of a signal peaking circuit for enhancing the high frequency signal response of the video driver circuitry in accordance with another embodiment of the present invention.

Figure 37 is a graph representing the high frequency signal enhancement characteristics of the circuit of Figure 36.

Figure 38 is a signal diagram illustrating the signal overshoot and increased slew rate introduced by the circuit of Figure 36.

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DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 6, the multiplexed video interface system 300 includes a monitor amplifier circuit AMP31-AMP33 for each video signal blue b, red r, and green g, and reduces the problems of the conventional monitor amplifier system 100. By integrating several of the components, multiplexed video interface system 300 can be constructed using only two integrated circuits (ICs) - a preamplifier circuit PREAMP and an output amplifier circuit OUTAMP. In an exemplary embodiment, preamplifier circuit PREAMP includes video preamplifiers 301a-301c and bias/brightness circuits 305-305c for each video signal blue b, red r, and green g, as well as switches SW31-SW36 and shared reference supply VSHR. It will be appreciated that although output buffers BUFF31-BUFF33 are illustrated in Figure 6, such use of output buffers BUFF31-BUFF33 is optional. If output buffers BUFF31-BUFF33 are used, they too may be integrated into preamplifier circuit PREAMP. In another exemplary embodiment, output amplifier OUTAMP includes video amplifiers 303a-303c and clamp amplifiers 307a-307c for each video signal blue b, red r, and green g.

For exemplary purposes only video interface system 300 has been divided into amplifier circuits AMP31-AMP33. Since the amplifier circuits AMP31-AMP33 are identical in structure and operation, only the circuit operation of amplifier circuit AMP32 for the red video signal r will be discussed by referring to Figure 7.

As illustrated in Figure 7, and as indicated above, amplification circuit AMP32

includes preamplifier circuit PREAMP and output amplifier circuit OUTAMP. To control the signal communication between preamplifier circuit PREAMP and output amplifier circuit OUTAMP, multiplexed video interface system 300 uses a video interface VI with a low level of complexity. Such video interface VI defines a process in which the red video signal r, output from video preamplifier 301b, and a variable direct current (DC) blank pulse BP are multiplexed into a single signal, buffered by buffer amplifier BUFF32, and sent to output amplifier OUTAMP.

The operation of multiplexed video interface system 300 illustrated in Figure 7, is best explained in conjunction with the signal diagrams (A)-(E) illustrated in Figure 8. Beginning with the preamplifier circuit PREAMP side of the multiplexed video interface system 300 as shown in Figure 7, the amplification of red video signal r is controlled by a video clamp pulse VC and a single-throw switch SW32. Figure 8(C) illustrates the clamp pulse VC, which develops just following the horizontal synchronous pulse HP, as illustrated in Figure 8(A).

Referring again to Figure 7, when clamp pulse VC is high, switch SW32 is closed and a shared voltage reference VSHR is coupled to the noninverting input of video preamplifier 301b and to capacitor CAP32. This shared voltage reference VSHR is the potential reference level of the black region of an image. Thus, each time the CRT scans a horizontal line, capacitor CAP32 is charged to the black level reference voltage from shared reference voltage VSHR. In an exemplary embodiment, the shared reference voltage VSHR is 1.8 volts (V). Thus, since there is no red video signal r during the time that clamp pulse VC is high, as shown in Figure 8(B), and since video preamplifier 301b is DC coupled from input to output, an input black level voltage of 1.8V causes an output black level voltage of 1.8V. It will be appreciated that although video preamplifier 301b is illustrated as a unity gain amplifier, video preamplifier 301b may also be an increasing, decreasing or variable gain amplifier.

Figure 9 illustrates an alternate embodiment of the present invention in which preamplifier circuit PREAMP includes a feedback circuit 601. This exemplary embodiment includes a feedback circuit 601 which is an operational amplifier having an inverting input coupled to the output of video preamplifier 301b, a noninverting input coupled to the shared reference supply VSHR, and an output coupled to switch SW32. In this way, feedback circuit 601, can be used within the clamp system to ensure the black level output by video preamplifier 301b during the clamp period (i.e., the period in which

the clamp pulse VC signal is high) is 1.8 V in order to eliminate any DC offsets that may be present in video preamplifier 301b.

Referring now to Figure 7 and Figure 8(C), when video clamp pulse VC is low, switch SW32 opens and red video input signal r is applied directly to video preamplifier 301b. The red video signal r is amplified by, or passed through, the video preamplifier 301b, depending upon whether preamplifier 301b is an increasing, decreasing, unity or variable gain amplifier. In this exemplary embodiment since preamplifier 301b is a unity gain amplifier, the red output video signal is the same as the red input video signal r. This red output video signal r is then applied to one pole of a double pole switch SW35, which is controlled by a signal 31.

Signal 31, illustrated in Figure 8(D), represents a horizontal blanking pulse which operates the double-throw switch SW35. In a conventional monitor amplifier system 100 (Figure 1), double-throw switch SW14 was switching between the output of video preamplifier 101b and circuit ground. In contrast, double-throw switch SW35 switches between the output of video preamplifier 301b and bias/brightness circuit 305b. In this way, horizontal blanking pulse 31 controls whether the red output video signal r, illustrated in Figure 8(B), or a variable DC blank pulse BP, is input to output buffer BUFF32. Again, it will be appreciated that the use of output buffer BUFF32 in amplifier circuit AMP32 is optional. In addition, although output buffer BUFF32 is illustrated as a unity gain amplifier, it will be appreciated that output buffer BUFF32 may also be an increasing, decreasing or variable gain amplifier.

When horizontal blanking pulse 31 is high, switch SW35 couples to the output of video preamplifier 301b to conduct the red output voltage signal r. When horizontal blanking pulse 31 is low, switch SW35 couples to bias/brightness circuit 305b to conduct variable DC blank pulse BP. Both signals, red output video signal r and variable DC blank pulse BP, are multiplexed to form a multiplexed signal VMUX32 and as illustrated in Figure 8(E), buffered by output buffer BUFF32 and sent to output amplifier OUTAMP.

Although the processing of a single red output video signal r has been described, it will be appreciated that On Screen Display (OSD) video information may also be multiplexed with the red output video signal r information in the video preamplifier PREAMP stage. Also, video from any other alternative source, such as when two sources of video information are used, may be mixed and viewed on one screen.

On the output amplifier OUTAMP side of video interface VI, multiplexed signal

VMUX is demultiplexed into its respective red output video signal r and variable DC blank pulse BP. This demultiplexing operation is explained in conjunction with Figure 7, and Figure 10 which illustrates exemplary voltage levels of a multiplexed signal VMUX72 including on screen display (OSD) data, red output video signal r data and a variable DC blank pulse BP. As illustrated in Figure 10, in this exemplary embodiment, the shared reference voltage VSHR is 1.8V. Although the voltage level of applied red output video signal r can range from 1.8-3.0V, the typical black voltage level VBLACKTYP is between 1.8-1.9V. In addition, the typical white voltage level VWHITETYP is between 2.55-3.0V. Thus, typically red output video signal r ranges in magnitude from 1.9-2.55V. The voltage level of variable DC blank pulse BP, which is a variable amplitude signal, typically is between 0.9-1.8V. Thus, signals having voltage levels greater than 1.8V correspond to red output video signals r, and signals having voltage levels less than 1.8 V correspond to variable DC blank pulses BP. Using this formula, output amplifier OUTAMP of Figure 7 can properly process both red output video signals r and variable DC blank pulses BP.

Shared reference voltage VSHR, in addition to being input into video preamplifier 301b, is applied to the inverting input of video amplifier 303b and the noninverting input of clamp amplifier 307b. It will also be appreciated that, referring again to Figure 6, shared reference voltage VSHR is input into each preamplifier 301a-301c, each inverting input of video amplifier 303a-303c, and each noninverting input of clamp amplifier 307a-307c. Referring again to Figure 7, as indicated above, a comparison of this shared reference voltage VSHR, will determine which of the two amplifiers 303b, 307b process red output video signal r, and which of the two amplifiers 303b, 307b process variable DC blank pulse BP.

Video amplifier 303b receives multiplexed signal VMUX32 at the noninverting input and shared reference voltage VSHR at the inverting input. When the magnitude or signal level of multiplexed signal VMUX transcends shared reference voltage VSHR in a first direction, for example, is greater than shared reference voltage VSHR, which is 1.8V in this example, video amplifier 303b amplifies this signal portion of the multiplexed signal VMUX32 to provide an amplified red video signal R. When the signal level of multiplexed signal VMUX32 transcends shared reference voltage VSHR in a second direction, for example, is less than shared reference voltage VSHR, video amplifier 303b is in saturation and therefore, inactive. In this way, only red output video signal r, which is

greater than 1.8V, is amplified by video amplifier 303b and sent to the CRT cathode.

In contrast, clamp amplifier 307b receives the multiplexed signal VMUX32 at the inverting input and shared reference voltage VSHR at the noninverting input. When the signal level of multiplexed signal VMUX32 transcends shared reference voltage VSHR in a first direction, for example, is greater than shared reference voltage VSHR, clamp amplifier 307b is in saturation and therefore, inactive. When the signal level of multiplexed signal VMUX32 transcends shared reference voltage VSHR in a second direction, for example, is less than shared reference voltage VSHR, clamp amplifier 307b amplifies this signal portion of the multiplexed signal VMUX32. In this way, only the variable DC blank pulse BP, which is less than 1.8V, is output from clamp amplifier 307b and sent to the CRT cathode.

Referring again to Figure 6, each of the other amplifiers circuits AMP31 and AMP33 operate like amplifier circuit AMP32, to amplify blue video signal b and green video signal g, respectively. In particular, amplifier circuit AMP31 includes video preamplifier 301a, bias/brightness circuit 305a, video amplifier 303a, clamp amplifier 307a, and optionally buffer amplifier BUFF31. Similarly, amplifier circuit AMP33 includes video preamplifier 301c, bias/brightness circuit 305c, video amplifier 303c, clamp amplifier 307c, and optionally buffer amplifier BUFF33. In an exemplary embodiment video preamplifiers 301a, 301c and bias/brightness circuits 305a, 305c are integrated with video preamplifier 301b, 305b in preamplifier circuit PREAMP. If used, buffer amplifiers BUFF31-BUFF33 are also integrated into preamplifier circuit PREAMP. Clamp amplifiers 307a, 307c and video amplifiers 303a, 303c are integrated with clamp and video amplifiers 307b, 303b in output amplifier circuit OUTAMP.

The amplification of both the blue and green video signals b, g is controlled by video clamp pulse VC and corresponding single-throw switch SW31, SW33. Thus, when clamp pulse VC is high, switches SW31, SW33 close to charge the respective capacitor CAP31, CAP33 while the corresponding video preamplifier 301a, 301c outputs the black level voltage of shared reference voltage VSHR. On the other hand, when clamp pulse VC is low, the blue and green video signals b, g pass through the video preamplifiers 301a, 301c, respectively.

Similar to operation of amplifier circuit AMP32, horizontal blanking pulse 31 controls double-throw switches SW34 and SW36, to switch between video preamplifier 301a, 301c and bias/brightness circuit 305a, 305c. For example, the switching operation

by switch SW34, causes blue video signal b to be mixed with the output from bias/brightness circuit 305a, which is a variable DC blank pulse BP, resulting in a multiplexed signal VMUX31 which is sent to output amplifier circuit OUTAMP. Similarly, the switching operation by switch SW36 causes the green video signal g to be mixed with the output signal from bias/brightness circuit 305c, which is also a variable DC blank pulse BP, forming a multiplexed signal VMUX33 which is sent to output amplifier circuit OUTAMP.

Clamp and video amplifiers 307a, 307c, 303a, 303c of output amplifier circuit OUTAMP demultiplex the multiplexed signals VMUX31, VMUX33 in the same way as clamp and video amplifiers 307b, 303b to provide the amplified video signals B, G and variable DC blank pulses to the CRT cathode.

Referring now to Figure 11, an exemplary DC input/output (I/O) transfer characteristic for video and clamp amplifiers 303b, 307b is shown. In this embodiment, shared reference voltage VSHR is again 1.8V, voltage supply VCC1 for video amplifier 303b is 80V, and voltage supply VCC2 for the clamp amplifier 307b is 120V. The x-axis represents the input voltage amplitude of multiplexed signal VMUX32. The y-axis represents the output voltage of signals from video and clamp amplifiers 303b, 307b. In this example, the active clamp dynamic input range CIN for clamp amplifier 307b is 0.9-1.75V, as illustrated by double arrow 81, whereas the active dynamic video input range VIN for video amplifier 303b is 1.9-3.0V, as illustrated by double arrow 82. The active clamp dynamic output COUT range for clamp amplifier 307b is 65-115V, as illustrated by double arrow 83, whereas the active video dynamic output VOUT range for video amplifier 303b is 75-20V, as illustrated by double arrow 84.

There are several advantages to the multiplexed video interface system 300 as compared to conventional monitor amplifier system 100 (Figure 1). First, conventional low pin count packages can be used, thus reducing the cost of the video channel components. For example, the clamp video 303b and the amplifier 307b and the video driver amplifier 313a can be contained within a conventional 15 pin IC package such as the TO220 IC package. Also, preamplifier circuit PREAMP may be packaged with other functions, such as, an on-screen display generator, a digital communication bus circuit, and digitally controlled digital-to-analog converter (DAC) circuits, and still be contained in a small footprint and low cost Dual In Line (DIL) package.

Another advantage of the multiplexed video interface system 300 is the reduction in

the number of required IC connections, thus reducing the size and cost of the printed circuit boards (PCB). The smaller PCB size allows for closer connection of video preamplifier 301b to video amplifier 303b, thereby improving signal performance and reducing electromagnetic interference (EMI). EMI is further reduced because the video signal interface between preamplifier 301b and video amplifier 303b is approximately 12 decibels (dB) lower.

Finally, in one embodiment, the video amplifier 303b and clamp amplifier 307b are both differential amplifiers, and thus have good common mode noise rejection. In addition, the multiplexed interference signal is referenced to a stable and accurate voltage generated in the preamplifier. Thus, common mode noise and voltage variations in the system, such as the thermal drift or production variation that may occur in any of the circuits, are minimized.

Referring to Figure 12, a multiplexed video signal interface system 700 in accordance with one embodiment of the present invention includes two integrated circuits: a pre-amplifier 702 and CRT driver 704. As inputs, the pre-amplifier 702 receives: the component video signals 701b, 701g, 701r; a clamp signal 701c; an automatic beam limiting control signal 701a; horizontal 701h and vertical 701v blanking signals; and digital control signals 701i in accordance with the I2C standard. As output signals, the pre-amplifier 702 provides: clamped and amplified component video signals 703b, 703g, 703r; a reference DC voltage 703vr; and a buffered vertical blanking signal 703vb. Internally, the pre-amplifier 702 provides for amplifying and clamping the component video signals, as well as providing for individual control of gain, contrast, bias and brightness, with bias and brightness control information being multiplexed within the output component video signals 703b, 703g, 703r. Additionally, the pre-amplifier 702 provides for OSD character generation and mixing within the outgoing component video signals 703b, 703g, 703r.

The CRT driver 704, in accordance with the reference voltage 703vr and vertical blanking signal 703vb, further amplifies the component video signals 703b, 703g, 703r. The resulting amplified video signals 705b, 705g, 705r are clamped in a simple output clamping circuit 706 using DC clamp signals 705cr, 705cg, 705cb generated within the CRT driver 704. Additionally, the CRT driver 704 provides a grid signal 705vb for driving grid one of the CRT.

Internal to the CRT driver 704, the vertical blanking signal 703vb is used to generate

the necessary boosted high voltage for the DC clamping function, as well as for the amplifiers performing the demultiplexing function upon the multiplexed component video signals 703b, 703g, 703r (discussed in more detail below).

Referring to Figure 13, one video channel of the system of Figure 12 is shown in more detail. The incoming video signal 701vi is terminated with a termination resistor Rt for impedance matching purposes and is AC-coupled with a coupling capacitor Ci. The resulting AC-coupled signal 701b/g/r is DC-clamped by a clamping circuit 710 in accordance with the reference voltage 707vr, the horizontal clamp signal 701c and a voltage level fed back from a subsequent portion of the circuit (discussed in more detail below).

The DC-clamped signal 711 is then processed by a contrast controller 712 in accordance with contrast control signals 707c and the reference voltage 707vr. This allows the user to control the contrast of the video information via the contrast control signals 707c (discussed in more detail below).

The contrast-controlled signal 713 is then processed by an auto beam limit circuit 714 (various forms of which are well known in the art) in accordance with the ABL control signal 701a.

The resulting video signal 715 is fed back to the clamp circuit 710 (discussed in more detail below) and to a switch/multiplexor circuit 716 which is used to multiplex this video signal 715 and an OSD data signal 707od in accordance with an OSD enable control signal 707oe. The output signal 717 contains OSD and video information during the time intervals that the OSD control signal 707oe is asserted and de-asserted, respectively.

The resulting video/OSD signal 717 is then controlled with respect to signal gain by a video gain controller 718 in accordance with the reference voltage 707vr and gain control signals 707g (discussed in more detail below).

The resulting signal 719, which has now been DC-clamped, controlled for video contrast, controlled for beam signal strength, combined with OSD information and controlled for video gain, is multiplexed with a signal 721 containing brightness and bias control information in a switch/multiplexor circuit 728 controlled by the horizontal blanking signal 701h.

Digital brightness 707br and bias 707bi control signals are converted to their analog equivalent signals 723, 725 by digital-to-analog converter (DAC) circuits 722, 724. These analog signals 723, 725 are summed in a signal summing circuit 726 and the resulting sum

signal 727 and analog bias control signal 725 are processed in a brightness gain controller 720 in accordance with the gain control signals 707g to produce the signal 721 containing the brightness and bias control information (discussed in more detail below).

The resulting multiplexed signal 703b/g/r contains a video component with user-controlled contrast and gain, an OSD component with user-controlled gain, a brightness control component and a CRT bias control component (discussed in more detail below.) This signal 703b/g/r is demultiplexed and amplified by the driver amplifier 730 within the corresponding channel 704a of the CRT driver 704. This produces the video 731v and clamping 731c signals, which are combined in the clamping circuit 706a, needed to produce an appropriately clamped video signal 733b/g/r for the CRT.

In accordance with another embodiment of the present invention, as an alternative implementation, the circuitry of Figure 13 could be simplified by eliminating the brightness and bias control elements 722, 724, 726, 720. In such an implementation, signal 721 would simply be a reference voltage, e.g., circuit ground potential GND, thereby causing signal 719 to be multiplexed with such reference potential. This would allow controls over the brightness of the display and the bias of the CRT to be exercised by the user in other ways, as desired.

Referring to Figure 14, the multiplexing of the video input 701b/g/r and OSD data 707od during the active period of the signal can be better understood. As shown, the OSD data is inserted within the appropriate area of the video signal so as to place the OSD information in the desired position within the displayed image. During the horizontal blanking intervals, as defined by the horizontal blanking signal 701h, bias and brightness control information is provided.

Referring to Figure 15, the contrast control provided by the contrast controller 712 (Figure 13) can be better understood. As shown, the contrast control information 707c provides for the full range of contrast control between maximum and minimum white levels during the active period of the video signal. Also as shown, the level of the OSD information is unaffected since it is introduced into the video signal channel at a later point.

Referring to Figure 16, the gain control provided by the video gain controller 718 (Figure 13) over the video and OSD information can be better understood. As shown, both video and OSD information are affected with full control provided between maximum and minimum white levels. Additionally, as shown, this gain control also

affects the range of brightness control due to the use of the gain control signals 707g to control the brightness gain controller 720 (Figure 13).

Referring to Figure 17, the bias control for controlling the bias of the CRT in accordance with the bias control information 707bi (Figure 13) can be better understood. As shown, the bias control information 707bi sets the bias level without affecting the levels of the video, OSD or brightness components.

Referring to Figure 18, the resulting multiplexed video signal 703b/g/r is shown with the typical voltage levels associated with the typical, minimum and maximum levels of the various components of the multiplexed signal 703b/g/r.

As will be readily appreciated, such a multiplexed video signal 703b/g/r can be conveyed via any form of signal transmission medium, such as electrical conductors or fiberoptic media, as well as via wireless signal transmission techniques, such as electromagnetic (e.g., radio frequency) or infrared signals. Further, such a multiplexed video signal 703b/g/r can be advantageously preserved for later use via recordation on any form of recording medium. For example, such a signal can be recorded in electrical memory circuits, on magnetic disk or tape, or on printed media such as an optical disc (e.g., compact disc or digital video/versatile disc).

Referring to Figure 19, a preferred implementation 710a of the clamping circuit 710 (Figure 13) is represented. During a portion of the horizontal blanking interval, the horizontal clamp signal 701c is active and closes switch 754. This causes the DC voltage 753 from a comparator circuit 752 to be inserted into the signal path of the incoming AC-coupled video signal 701b/g/r. This DC voltage 753 is generated in accordance with the relative values of the reference voltage 707vr and the DC voltage level in the signal 715 at the output of the auto beam limit circuit 714 during the horizontal clamping time interval. The resulting DC-clamped video signal is buffered by a buffer amplifier 756 to produce the video signal 711 to be processed by the contrast controller 712 (as discussed above).

Referring to Figures 20 and 21, the demultiplexing of the multiplexed video signal 703b/g/r within each channel 704a of the CRT driver 704 can be better understood. It is performed using two comparator circuits 762, 764. In each circuit 762, 764, the incoming multiplexed video signal 703b/g/r is compared to the DC reference voltage 707vr. The video circuit 762, biased by the 80 volt power supply potential, produces an active output video signal 731v when the multiplexed video signal 703b/g/r is more positive than the

reference voltage 707vr, and produces a fixed DC level equal to the power supply potential when the multiplexed video signal 703b/g/r is more negative than the reference voltage 707vr. The clamping circuit 764, powered by a boosted high voltage source (discussed in more detail below), produces an active output clamp signal 765 when the multiplexed video signal 703b/g/r is more negative than the reference voltage 707vr, and produces a fixed output voltage equal to the boosted power supply potential when the multiplexed video signal 703b/g/r is more positive than the reference voltage 707vr. The clamp signal 765 is rectified by an output diode 766. The demultiplexed video signal 731v and rectified clamp signal 731c are then combined in the clamping circuit 706a (in accordance with well known techniques) to form an appropriately clamped video signal 733 for driving a cathode of the CRT.

Referring to Figure 22, the operation of the grid one blanking output signal 705vb (Figure 12) in combination with the generating of the boosted power supply voltage for the clamp circuit 764 (Figure 20) is illustrated.

Referring to Figure 23, a combined high voltage boost and blanking amplifier circuit in accordance with another embodiment of the present invention uses an amplifier 780 to amplify the vertical blanking pulse 703vb. This amplified blanking pulse 705vb has a typical peak-to-peak value of 40 volts (depending upon the boosted power supply potential required). This signal pulse 705vb is AC-coupled via capacitor C2 and connected to grid one of the CRT to provide the vertical blanking. The DC level of the voltage at grid one is restored through a resistor R1 connected to the DC power supply for grid one.

This output pulse 705vb (at node B) is also AC-coupled by capacitor C1 (to node A). Diode D1 clamps the lower portion of this pulse to just below the Vcc1 power supply potential (typically 80 volts) when the output pulse 705vb is in its low voltage state and causes capacitor C1 to become charged. When the amplifier 780 drives the pulse 705vb to its high voltage state, diode D2 is conductive and causes charge from capacitor C1 to be transferred to capacitor C3, thereby creating a power supply equal to the Vcc1 supply plus the amplitude of the blanking pulse (typically 80+40=120 volts).

Capacitor C3 (shunt connected to circuit ground) is optional and can be small in value due to the short duty cycle of the vertical blanking interval. Alternatively, the bias clamp circuits can simply use the voltage supplied directly via diode D2 from capacitor C1, provided that the bias clamp circuits are designed to be inactive during the vertical blanking interval (and thus not requiring any boosted power supply during the vertical

blanking interval).

Since the vertical blanking pulse 705vb has a short duty cycle, it is necessary that capacitor C1 store sufficient charge to supply the bias clamp circuits, thereby requiring capacitor C1 to be relatively large in value and, as a result, requiring high initial charging currents. To prevent damage during initial application of power, when capacitor C1 may not yet be charged, the output of the vertical blanking amplifier 780 must be current limited to a range defined by a maximum (e.g., positive) current value Imax and a minimum (e.g., negative) value of current Imin.

While this circuit implementation may be satisfactory in many instances, one disadvantage is that capacitor C1 may require many cycles to charge to its full value due to the short duty cycle of the vertical blanking pulse 705vb and the limited current output of the amplifier 780. Referring to Figure 24, this may cause an undesirable delay in achieving the full boosted power supply voltage required by the bias clamp amplifiers.

Referring to Figure 25, such undesirable start-up delays may be overcome using a vertical blanking circuit 780a in accordance with that shown. When the first vertical blanking input pulse 703vb is encountered at start-up, a latch circuit 782 holds the output 705vb low, thereby causing capacitor C1 to be discharged at the maximum current limit at Imax until the output drops below the low level threshold. At this point, the latch 782 is cleared. Normally, if the input 703vb has changed to the unblanked level, the output 705vb is then released, immediately causing capacitor C3 to become charged and thus producing the boosted power supply for the bias clamp circuits.

More specifically, a positive-going vertical blanking input pulse 703vb simultaneously sets the latch 782 and drives one input to an OR gate 786. The other input to the OR gate 786 is provided by the Q output of the latch 782. The output 787 of the OR gate 786 drives a switch 788 which switches the output of the amplifier 780 to a predetermined low voltage level Vlow.

This output voltage 705vb is also connected to the input of a comparator circuit 784. As long as the input signal 703vb is high, then the switch 788 is connected to the low voltage Vlow. If the input signal 703vb goes low and the output 783 of the latch 782 is also low, then the switch 788 connects to a high voltage level Vhigh, thereby driving the output signal 705vb to a high voltage level Vhigh. However, if the output voltage 705vb has not dropped below the reference voltage 703vr before the input signal 703vb has gone low, then the output 783 of the latch 782 holds the switch 788 in the Vlow position until

the output 705vb does drop below the reference voltage 703vr. At that point, the latch 782 is reset and the switch 788 is switched to the high voltage position Vhigh. (As a practical matter, the reference voltage 703vr is generally only slightly higher than the low voltage potential Vlow, thereby ensuring that the latch 782 is only reset when practically the full swing of the voltage has been achieved at the output 705vb.)

Referring to Figure 26, it can be seen that the boost capacitor C3 is charged quickly after the first vertical blanking pulse 703vb is received. This ensures that the boosted power supply potential (120 volts DC) is created in a very short time of one or two vertical scan intervals.

Referring to Figure 27, one implementation 780b of the circuit of Figure 25 is shown in more detail and operates substantially as follows. Transistors Q1, Q2, and Q3 provide an intermediate power supply (approximately 45 volts) to set the high level of the output pulse. The input pulse 703vb drives the base of transistor Q4. Transistors Q5 and Q6 form a latching circuit. When the input pulse 703vb goes high and the output is in a high voltage state, transistors Q5 and Q6 latch to pull the base of transistor Q5 high, thereby ensuring that transistor Q5 remains turned on regardless of subsequent changes in the level of the input pulse 703vb.

When transistor Q5 is turned on, transistor Q7 is also turned on. In turn, this causes transistor Q12 to be turned on. Also, with transistor Q5 turned on, transistor Q8 is turned off, thereby turning off transistor Q10 through the current mirror action of transistor Q9.

With transistor Q7 turned on, transistor Q12 acts like a constant current source, thereby discharging the output node 781. Eventually, the output voltage drops in value so that the base-collector junction of transistor Q11 is forward biased. As the output voltage drops further, the emitter of transistor Q6 is pulled down, thereby clearing the latch formed by transistors Q5 and Q6. If the input pulse 703vb is in a high voltage state, then transistor Q5 remains on due to the base drive provided by transistor Q4. In that case, the output reaches its lower voltage level set by the current limit within transistor Q12 and the voltage developed by the current flowing through transistor Q11 and resistor R270. If the input voltage 703vb is low when the latch is cleared, then transistor Q5 turns off and, in turn, transistor Q12 turns off. Transistor Q8 is now turned on and the collector current of transistor Q8 is mirrored by transistor Q9 and amplified by transistor Q10 to provide the current limited pull-up drive to pull the output node 781 to a high voltage level.

Control circuits suitable for use as the contrast controller 712, video gain controller

718 and brightness gain controller 720 are disclosed in U.S. Patent application No. 09/348,533, filed July 7, 1999, and entitled "Digitally Controlled Signal Magnitude Control Circuit" (incorporated herein by reference), as follows.

Referring to Figure 28, an analog signal system using a digitally controlled signal magnitude control circuit in accordance with one embodiment of the present invention includes a magnitude control circuit 10, buffer amplifiers 12, 14, a DC reference voltage source 16, a synchronous switching circuit 18 and a series coupling capacitor 20. The input signal 25, which typically includes both AC and DC signal components, is AC-coupled to node 22 where it is summed with the DC reference voltage 17, via the switch circuit 18, during the DC clamping intervals as defined by the clamp signal 23 (e.g., such as during the horizontal blanking interval in the case of a video input signal). This DC-clamped signal 21 is buffered by the buffer amplifier 12. The DC reference voltage 17 is also buffered by a buffer amplifier 14.

These buffered composite (i.e., AC and DC) 13 and DC 15 signals are provided to the magnitude control circuit 10. In accordance with a digital control signal 9, the output signal 11 is another composite signal. This signal 11 includes a DC component equal to the buffered DC reference voltage 15 (as well as the buffered DC component of the input composite signal 13). This signal 11 further includes an AC component which is equal to the buffered AC component of the input composite signal 13 multiplied by the transfer function of the stage 10 as determined by the digital control signal 9. (For example, if the digital control signal 9 defines an attenuation of 5 decibels, the AC component in the output signal 11 is 5 decibels less than the AC component of the input signal 13.)

Referring to Figure 29, the magnitude control circuit 10 of Figure 28 can be represented by the embodiment 10a which includes an input buffer amplifier 30 and a digitally controlled resistive attenuator circuit 32. The DC reference voltage 15 is applied at the bottom, while the buffered composite signal 31 is applied at the top. In accordance with the digital control signal 9, variable resistances 36a, 36b, 36c are adjusted, thereby producing, in conjunction with a series resistance 34, a resistive attenuation factor. (Specific and more detailed embodiments of this resistive circuit 32 are discussed in more detail below.)

Referring to Figure 30, operation of the circuit of Figure 28 when used to process a clamped video signal can be better understood. During the horizontal blanking interval, the DC reference voltage 17 (Figure 28) clamps the AC-coupled input signal. During the

active video or OSD (on screen display) portions of the input signal 25, the digital control signal 9 determines the attenuation of the buffered composite signal 13 to establish the level of the output signal 11. In this example, for a 7-bit control signal 9, the output signal 11 can be adjusted over the range of 2.05 volts (maximum attenuation) through 3.0 volts (minimum attenuation).

Referring to Figure 31, in accordance with another embodiment of the present invention, the magnitude control circuit 10 can be used to process, in accordance with the reference voltage 15, a variable DC voltage signal 13. In the case of a video signal system, for example, this voltage 13 can be the brightness control for the display monitor. A digital input signal 47 is varied in value in accordance with the desired brightness setting. This signal 47 drives a digital-to-analog converter circuit (DAC) 42, thereby producing a variable analog voltage signal 43 which is buffered by the buffer amplifier 12 to drive the top of the magnitude control circuit 10. Similarly, the DC reference source can be implemented using another DAC 40, thereby allowing the DC reference voltage 15 to also be established in accordance with a digital control signal 45.

Referring to Figure 32, the effect of the digital control signal 9 upon the resulting variable DC output signal 11 from the circuit of Figure 31 can be better understood. For a minimum attenuation (or maximum gain) as defined by the digital control signal 9, the output signal 11 will vary between values A1 and B1 with a slope G1 as shown. Conversely, for a maximum attenuation (or minimum gain), the output signal 11 will vary over a range of A2 through B2 with a slope of G2 as shown. These ranges can be shifted up (more positive) or down (more negative) in accordance with the bias voltage BIAS which is established by the DC reference voltage 15. These ranges of values of the variable DC output signal 11, as compared to the corresponding ranges of values of the input variable DC voltage signal 13, are determined by the attenuation factor established by the digital control signal 9.

Referring to Figure 33, operation of the circuit of Figure 31 in a video signal system can be better understood. During the horizontal blanking interval, the brightness control range, as defined by the digital control signal 9, can be varied as shown. This control range, as noted above, can be shifted by varying the DC reference voltage in more positive or more negative directions. For example, for a DC reference, or bias, voltage of 1.3 volts (as established by the control signal 45 to the DC reference voltage source DAC 40) and a 400 millivolt brightness control voltage (as established by the brightness control

signal 47), the digital magnitude control signal 9 can vary the brightness control output signal 11 over a range of 1.1 volts (maximum attenuation) through 1.48 volts (minimum attenuation).

Referring to Figure 34, one embodiment 10b of the magnitude control circuit 10 (Figures 28 and 31) can be implemented as shown. The input buffer amplifier 30 is implemented as a complementary MOSFET amplifier 30a. As discussed above (in connection with Figure 29), the buffered signal 31 drives the top of the resistive array 32a, while the DC reference voltage 15 drives the bottom. Series-connected pass transistors in the form of P-type MOSFETs 50 and N-type MOSFETs 52 and a set of series resistances 54 are connected between the nodes driven by the signal 31 and reference voltage 15. (In this example, due to the integrated circuit structure being used, the various resistors 54, 56, 58 are implemented using MOSFET devices with fixed bias potentials (PWRP or PWRN, as appropriate) applied to their respective gate terminals.)

In accordance with the binary states of the bits A0-A6 (in this case 7 bits) of the digital control signal 9a, the pass transistors 50, 52 cause the bottom ends of resistor circuits 56 to be driven by either the buffered signal 31 or the reference voltage 15. This has the effect of connecting various permutations of series resistors 58 and shunt resistors 56 across either the upper portion 54a or lower portion 54b of the shunt resistive circuit 54 on the input side. The resulting net resistance interacts with the series fixed resistance 34a to produce the desired attenuation factor. This selective connecting of the various resistances in this manner produces the variable resistances 36a, 36b, 36c depicted in the circuit diagram of Figure 29.

Referring to Figure 35, another embodiment 10c of the magnitude control circuit 10 uses the same basic technique of switching resistances to produce the variable resistive network depicted in Figure 29, but uses transmission gate circuits 60, 62 in place of the pass transistors 50, 52. Accordingly, the individual bits A0-A5 (in this case 6 bits) of the digital control signal 9b are also inverted using inverter circuits 64 for driving the transmission gate circuits 60, 62. This circuit 32b operates in an manner similar to that of the circuit 32a of Figure 34. However, the transmission gate circuits 60, 62 provide improved isolation for when the incoming signal 31 is a variable DC voltage which may, at times, be more negative than the DC reference voltage 15. This allows the nodes driven by the signal 31 and reference voltage 15 to "flip" in polarity with respect to each other as needed. In other words, as shown in the graph of Figure 32, the output signal 11 may

sometimes be more negative than the DC reference voltage 15 providing the bias potential. Using transmission gate circuits 60, 62 allows this to be done more reliably.

Referring to Figure 36, in accordance with another embodiment of the present invention, the high frequency response of the video driver circuitry can be enhanced using the signal peaking circuit 770 as shown. Such circuit 770 would be coupled between the switch/multiplexor circuit 728 and driver amplifier 730 (see Figure 13) to perform a high pass filter function. The high frequency signal components of the multiplexed signal 703b/g/r are enhanced, or amplified, to produce a "peaked" multiplexed signal 773b/g/r for the driver amplifier 730 (see Figure 20).

As will be readily apparent, the operational amplifier 772 has a feedback circuit which is capacitive in nature due to the serial connection of feedback resistor R2 with the selective shunt connection of resistor R1 and capacitors 778a, 778b and 778c. A multibit control signal 771b determines which of the respective switches 776a, 776b, 776c (e.g., implemented in the form of pass transistors or transmission gates) is closed, thereby connecting the corresponding capacitor 778a, 778b, 778c. As more capacitors 778a, 778b, 778c are connected (three are used here but it will be readily apparent that any number can be used depending upon the desired signal peaking effects), the more (and the sooner in terms of frequency) the high frequency signal components of the multiplexed signal 703b/g/r become enhanced.

A digital-to-analog current source 774 is used to convert a multibit control signal 771a to an analog DC current signal I775 for injection at node 775, thereby affecting the voltage at the inverting terminal of the operational amplifier 772. This allows for controlling the resulting baseline, or reference, level of the peaked multiplexed signal 773b/g/r and is useful when the driver amplifier 730 uses a voltage reference ("Vref" in Figure 20) that is different from that reference voltage Vref used by the circuitry of Figure 13. Alternatively, of course, resistor R1 can be driven by a controlled voltage other than Vref to achieve the same effect.

Referring to Figure 37, using this circuit causes the higher frequency components of the video and OSD signal components to be emphasized with respect to the lower frequency components. Referring to Figure 38, as a result, the rising edge 779 of such signals would become steeper as such high frequency signal enhancement increased. For example, with increasing high frequency signal enhancement, the slope of rising edge 779 would increase from slope A through slope B to slope C, while the peak of the signal

would exhibit a corresponding extending from A through peak overshoot B to peak overshoot C.

Further information can be found in a product requirement specification, Appendix A attached hereto and incorporated herein by reference, and portions of a training manual, Appendix B attached hereto and incorporated herein by reference, for a chipset developed by the assignee National Semiconductor Corporation of Santa Clara, California.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

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WHAT IS CLAIMED IS:

1. An apparatus including a signal multiplexor for controlling and multiplexing video image and on-screen-display (OSD) signals, comprising:

a first control circuit that following reception of a first reference signal, a contrast control signal and a clamped video signal provides a first controlled signal with a contrast-controlled video component;

a first signal combining circuit, coupled to said first control circuit, that in response to a first combining control signal receives and selectively combines an OSD signal and said first controlled signal to thereby provide a first combination signal with said contrast-controlled video component and an OSD component;

a second control circuit, coupled to said first signal combining circuit, that following reception of said first combination signal, said first reference signal and a gain control signal provides a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component; and

a second signal combining circuit, coupled to said second control circuit, that in response to a second combining control signal receives and selectively combines said second controlled signal and a second reference signal to thereby provide a multiplexed signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component.

2. The apparatus of claim 1, further comprising a clamp circuit, coupled to said first control circuit, that following reception of said first reference signal, a clamp control signal, said first controlled signal and an input video signal provides said clamped video signal.

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3. The apparatus of claim 2, wherein said clamp circuit comprises:

an input stage that following reception and combination of a switched clamp signal and said input video signal provides said clamped video signal;

a comparator circuit, coupled to said first control circuit, that following reception and comparison of said reference signal and said first controlled signal provides a clamp signal; and

a switch circuit, coupled between said comparator circuit and said input stage, that in response to said clamp control signal receives and switches said clamp signal to thereby provide said switched clamp signal.

4. The apparatus of claim 1, wherein said first signal combining circuit comprises a multiplexor circuit that multiplexes said OSD signal and said first controlled signal in response to said first combining control signal to thereby provide said first combination signal.

5. The apparatus of claim 1, wherein said second signal combining circuit comprises a multiplexor circuit that multiplexes said second and third controlled signals in response to said second combining control signal to thereby provide said multiplexed signal.

6. A multiplexed signal containing controlled video image and on-screen-display (OSD) information, comprising:

a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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7. A multiplexed signal containing controlled video image and on-screen-display (OSD) information and conveyed via a signal medium, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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8. A multiplexed signal containing controlled video image and on-screen-display (OSD) information for conveyance via a signal medium, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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9. A method of controlling and multiplexing video image and on-screen-display (OSD) signals, comprising the steps of:

receiving a first reference signal, a contrast control signal and a clamped video signal and in response thereto generating a first controlled signal with a contrast-controlled video component;

receiving a first combining control signal and in response thereto receiving and selectively combining an OSD signal and said first controlled signal and thereby generating a first combination signal with said contrast-controlled video component and an OSD component;

receiving said first combination signal, said first reference signal and a gain control signal and in response thereto generating a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component; and

receiving a second combining control signal and in response thereto receiving and selectively combining said second controlled signal and a second reference signal and thereby generating a multiplexed signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component.

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10. A multiplexed signal recorded on a recording medium and containing controlled video image and on-screen-display (OSD) information, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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11. A recording medium having recorded thereon a multiplexed signal containing controlled video image and on-screen-display (OSD) information for controlling a display of said video image, said recording medium having been prepared by the steps of:

recording a contrast-controlled and gain-controlled video component representing a portion of a video image for display as a portion of a composite display image on a display device;

recording a gain-controlled OSD component representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

recording a reference component representing a blanked portion of said composite display image on said display device.

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12. An apparatus including a signal multiplexor for controlling and multiplexing video image and on-screen-display (OSD) signals, comprising:

a first control circuit that following reception of a first reference signal, a contrast control signal and a clamped video signal provides a first controlled signal with a contrast-controlled video component;

a first signal combining circuit, coupled to said first control circuit, that in response to a first combining control signal receives and selectively combines an OSD signal and said first controlled signal to thereby provide a first combination signal with said contrast-controlled video component and an OSD component;

a second control circuit, coupled to said first signal combining circuit, that following reception of said first combination signal, said first reference signal and a gain control signal provides a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component;

a second signal combining circuit, coupled to said second control circuit, that in response to a second combining control signal receives and selectively combines said second controlled signal and a second reference signal to thereby provide a multiplexed signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component; and

a variable filter circuit, coupled to said second signal combining circuit, that in response to a plurality of filter control signals selectively filters said multiplexed signal to thereby provide a filtered multiplexed signal with said contrast-controlled and gain-controlled video component and said gain-controlled OSD component having enhanced high frequency signal magnitudes.

13. The apparatus of claim 12, further comprising a clamp circuit, coupled to said first control circuit, that following reception of said first reference signal, a clamp control signal, said first controlled signal and an input video signal provides said clamped video signal.

14. The apparatus of claim 13, wherein said clamp circuit comprises:

an input stage that following reception and combination of a switched clamp signal and said input video signal provides said clamped video signal;

a comparator circuit, coupled to said first control circuit, that following reception and comparison of said reference signal and said first controlled signal provides a clamp signal; and

a switch circuit, coupled between said comparator circuit and said input stage, that in response to said clamp control signal receives and switches said clamp signal to thereby provide said switched clamp signal.

15. The apparatus of claim 12, wherein said first signal combining circuit comprises a multiplexor circuit that multiplexes said OSD signal and said first controlled signal in response to said first combining control signal to thereby provide said first combination signal.

16. The apparatus of claim 12, wherein said second signal combining circuit comprises a multiplexor circuit that multiplexes said second and third controlled signals in response to said second combining control signal to thereby provide said multiplexed signal.

17. The apparatus of claim 12, wherein said variable filter circuit comprises a variable high pass filter circuit.

18. The apparatus of claim 12, wherein said variable filter circuit comprises:

an amplifier circuit; and

a variably capacitive feedback circuit, coupled to said amplifier circuit, that in response to a portion of said plurality of filter control signals provides a variably capacitive feedback for said amplifier circuit.

19. The apparatus of claim 18, wherein said variably capacitive feedback circuit comprises:

a plurality of capacitive circuit elements;

a plurality of switch circuits, coupled between said amplifier circuit and said plurality of capacitive circuit elements, that in response to said portion of said plurality of filter control signals selectively provide electrical connections between said amplifier circuit and said plurality of capacitive circuit elements.

20. The apparatus of claim 18, further comprising a variable DC signal generator circuit, coupled to said variable filter circuit, that in response to another portion of said plurality of filter control signals provides a variable DC signal to said variably capacitive feedback circuit.

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21. A multiplexed signal containing controlled video image and on-screen-display (OSD) information, comprising:

a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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22. A multiplexed signal containing controlled video image and on-screen-display (OSD) information and conveyed via a signal medium, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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23. A multiplexed signal containing controlled video image and on-screen-display (OSD) information for conveyance via a signal medium, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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24. A method of controlling and multiplexing video image and on-screen-display (OSD) signals, comprising the steps of:

receiving a first reference signal, a contrast control signal and a clamped video signal and in response thereto generating a first controlled signal with a contrast-controlled video component;

receiving a first combining control signal and in response thereto receiving and selectively combining an OSD signal and said first controlled signal and thereby generating a first combination signal with said contrast-controlled video component and an OSD component;

receiving said first combination signal, said first reference signal and a gain control signal and in response thereto generating a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component;

receiving a second combining control signal and in response thereto receiving and selectively combining said second controlled signal and a second reference signal and thereby generating a multiplexed signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component; and

receiving a plurality of filter control signals and in response thereto selectively filtering said multiplexed signal and thereby generating a filtered multiplexed signal with said contrast-controlled and gain-controlled video component and said gain-controlled OSD component having enhanced high frequency signal magnitudes.

25. A multiplexed signal recorded on a recording medium and containing controlled video image and on-screen-display (OSD) information, said multiplexed signal comprising:

a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

a reference component representing a blanked portion of said composite display image on said display device.

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26. A recording medium having recorded thereon a multiplexed signal containing controlled video image and on-screen-display (OSD) information for controlling a display of said video image, said recording medium having been prepared by the steps of:

recording a contrast-controlled and gain-controlled video component having enhanced high frequency signal magnitudes and representing a portion of a video image for display as a portion of a composite display image on a display device;

recording a gain-controlled OSD component having enhanced high frequency signal magnitudes and representing a portion of an OSD image for display as another portion of said composite display image on said display device; and

recording a reference component representing a blanked portion of said composite display image on said display device.

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ABSTRACT OF THE DISCLOSURE

A multiplexed video signal interface in accordance with the present invention provides a multiplexed component video signal which includes component video signals with OSD data and user-controllable contrast and video gain, along with the ability to individually control such signal components. This advantageously minimizes the complexity of the necessary signal interfaces and allows for greater integration of circuit functions, thereby significantly reducing circuit complexity, size and costs. Also provided is a signal peaking circuit in the form of a variable high pass filter that enhances the magnitudes of the higher frequency signal components of the component video signals and OSD data, thereby providing for sharper edges on the displayed images.

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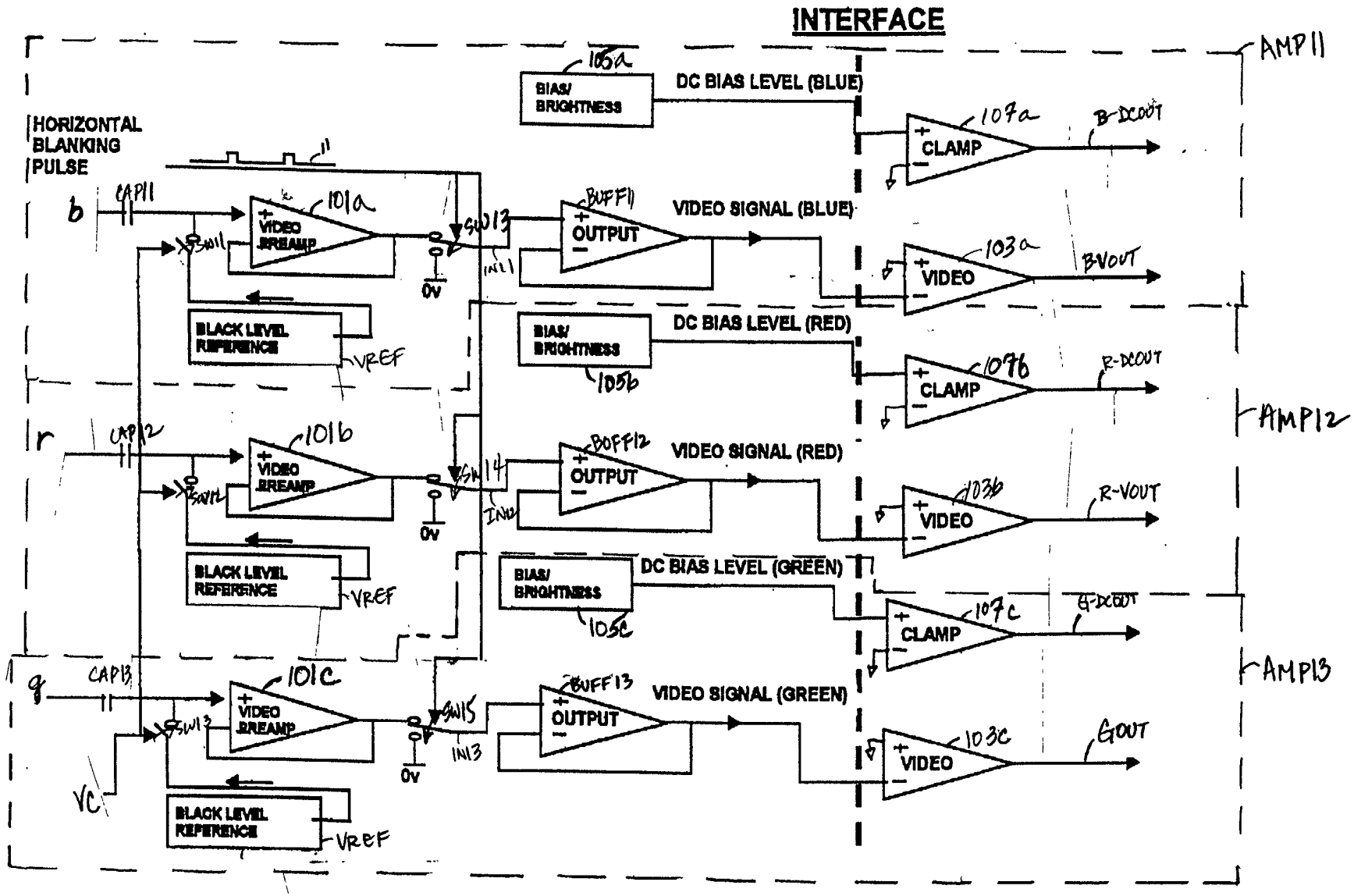
INTERFACE
AMP11
AMP12
AMP13
HORIZONTAL BLANKING PULSE
b
r
g
CAP11
CAP12
CAP13
101a
101b
101c
VIDEO PREAMP
SW11
SW12
SW13
SW14
SW15
0v
BLACK LEVEL REFERENCE
VREF
VC
105a
105b
105c
BIAS/ BRIGHTNESS
DC BIAS LEVEL (BLUE)
DC BIAS LEVEL (RED)
DC BIAS LEVEL (GREEN)
BUFF11
BUFF12
BUFF13
OUTPUT
VIDEO SIGNAL (BLUE)
VIDEO SIGNAL (RED)
VIDEO SIGNAL (GREEN)
107a
107b
107c
CLAMP
B-DCOUT
R-DCOUT
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103a
103b
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VIDEO
B-VOUT
R-VOUT
G-VOUT

100

FIGURE 1

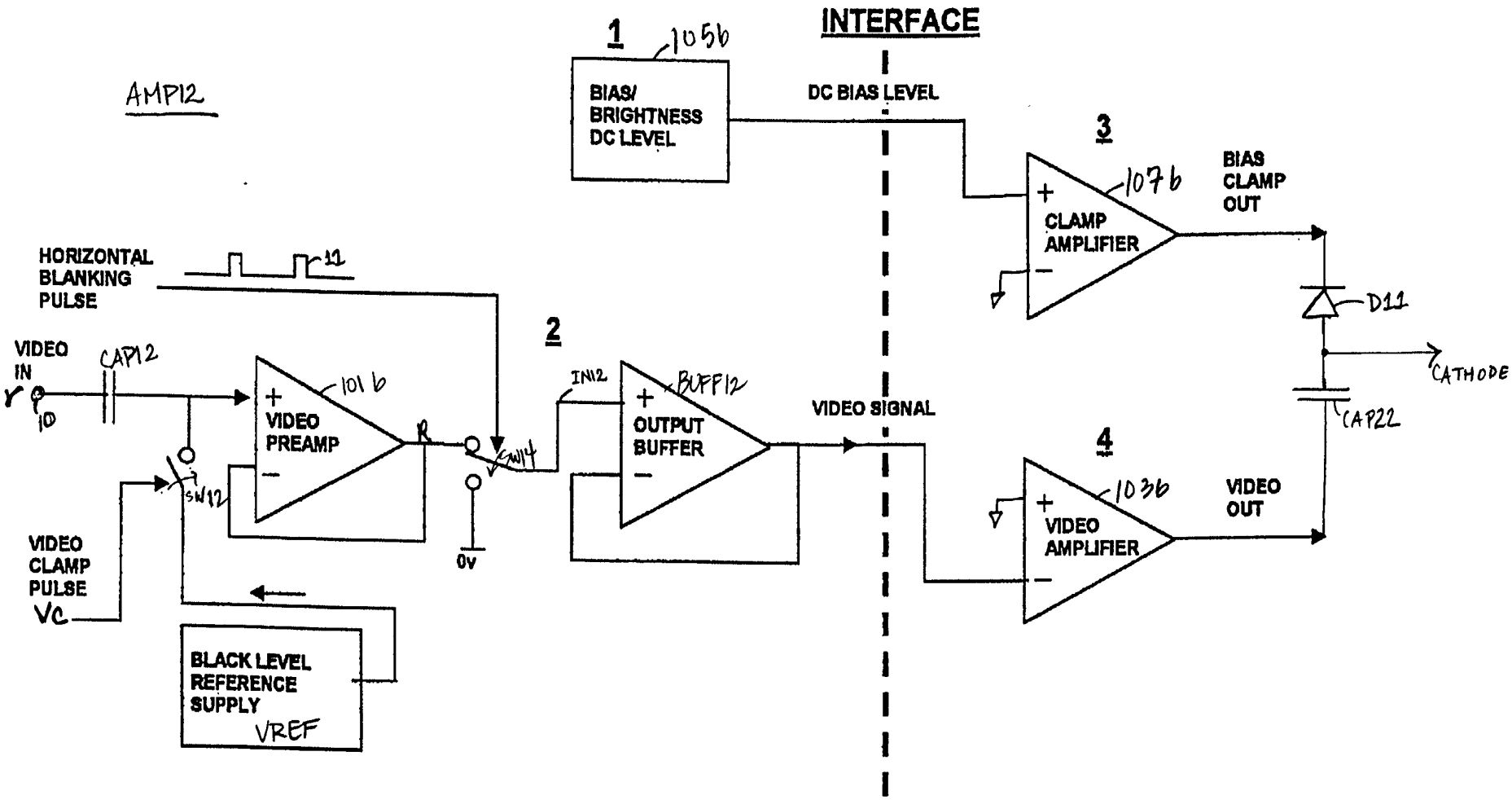
AMP12
INTERFACE
1
105b
BIAS/
BRIGHTNESS
DC LEVEL
DC BIAS LEVEL
3
107b
CLAMP
AMPLIFIER
BIAS
CLAMP
OUT
D11
CATHODE
CAP22
HORIZONTAL
BLANKING
PULSE
11
VIDEO
IN
10
CAP12
2
101b
VIDEO
PREAMP
R
SW14
IN12
BUFF12
OUTPUT
BUFFER
VIDEO SIGNAL
4
103b
VIDEO
AMPLIFIER
VIDEO
OUT
SW12
0V
VIDEO
CLAMP
PULSE
Vc
BLACK LEVEL
REFERENCE
SUPPLY
VREF

FIGURE 2

National Semiconductor

AG2DC

TYPICAL DISPLAY VIDEO SYSTEM

ARC PROTECTION, ESD, INPUT TERMINATION ETC NOT SHOWN

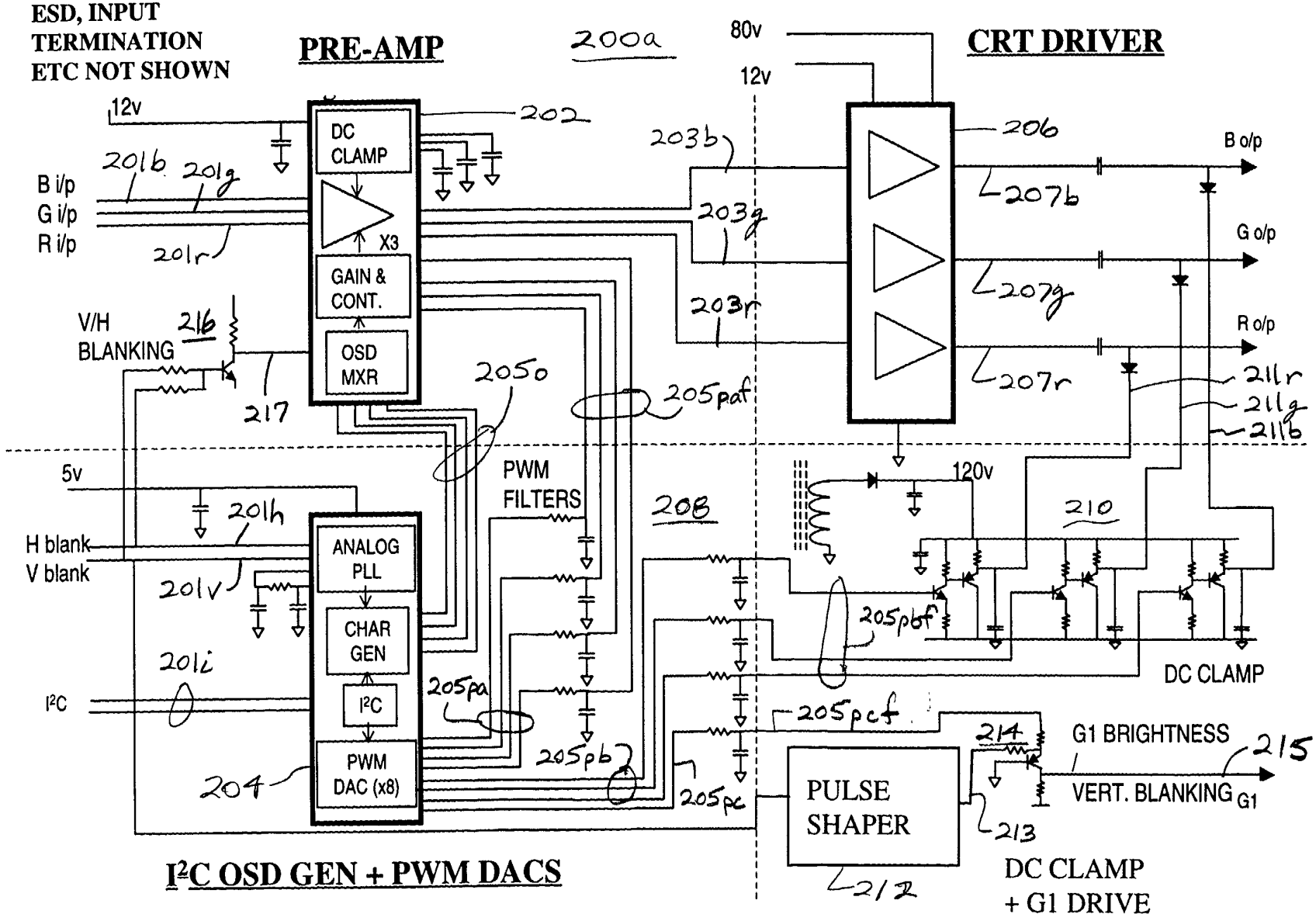

FIGURE 3 (PRIOR ART)

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National Semiconductor

AC2DC

DC COUPLED VIDEO SYSTEM

ARC PROTECTION, ESD, INPUT TERMINATION ETC NOT SHOWN

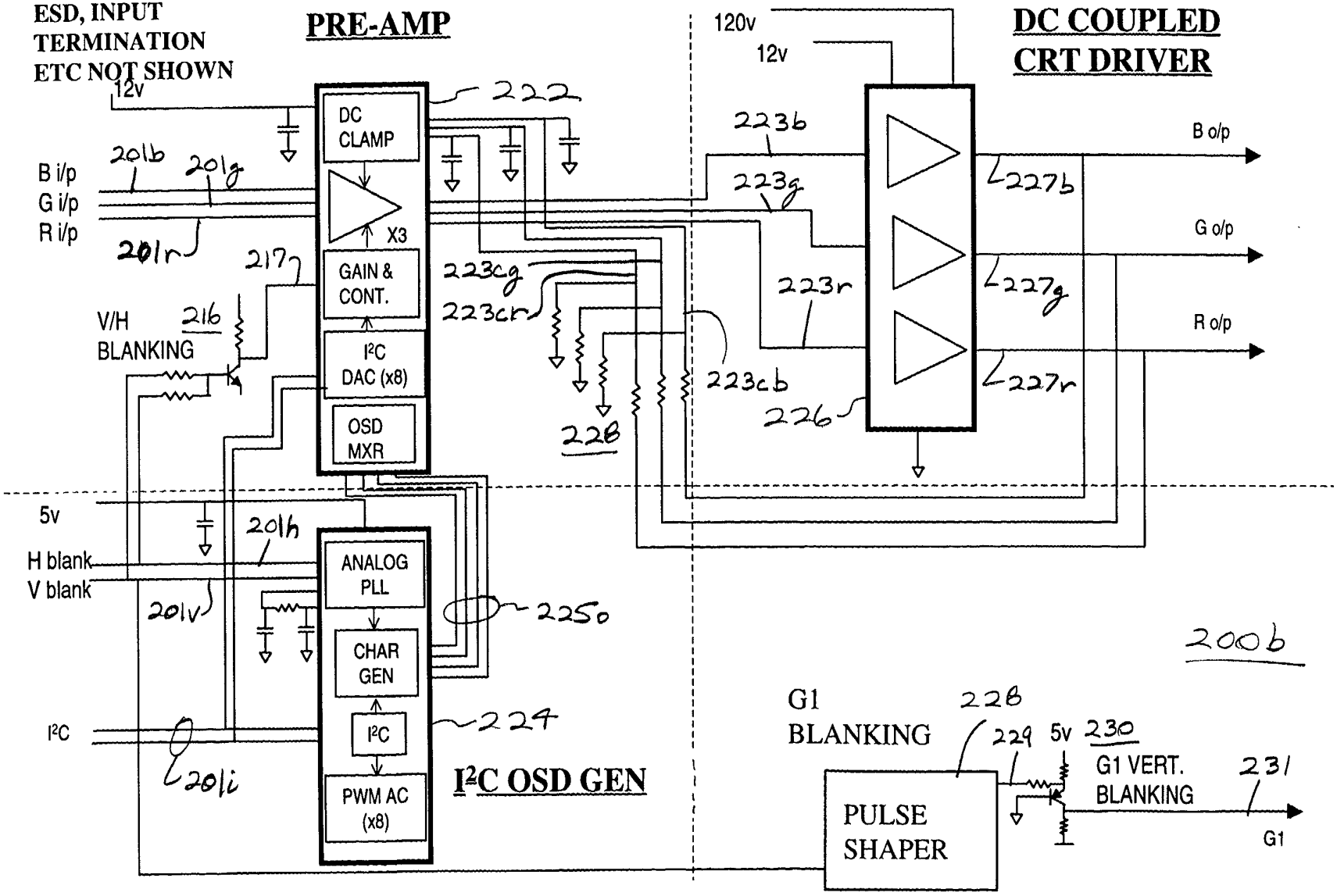

FIGURE 4 (PRIOR ART)

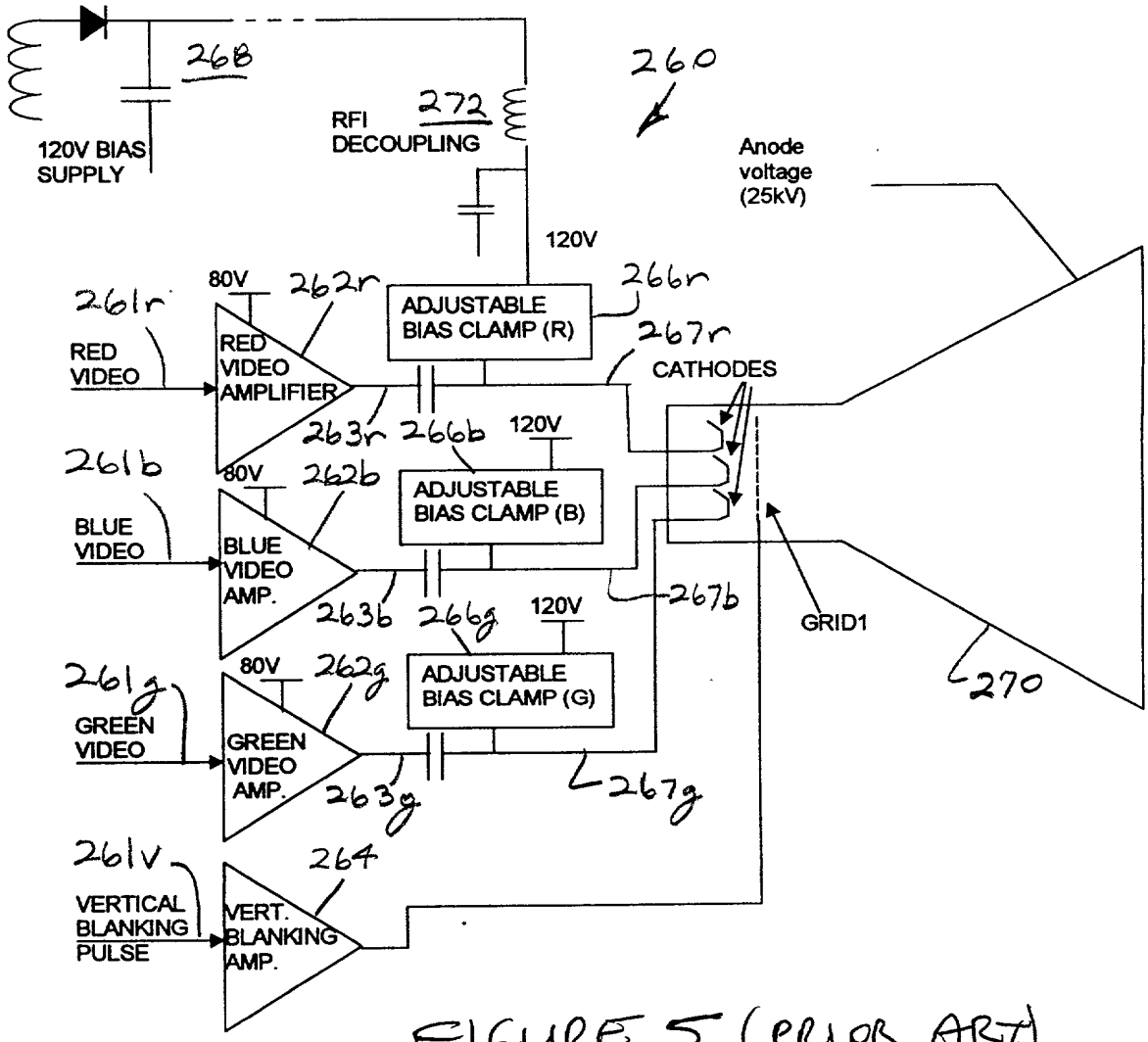

FIGURE 5 (PRIOR ART)

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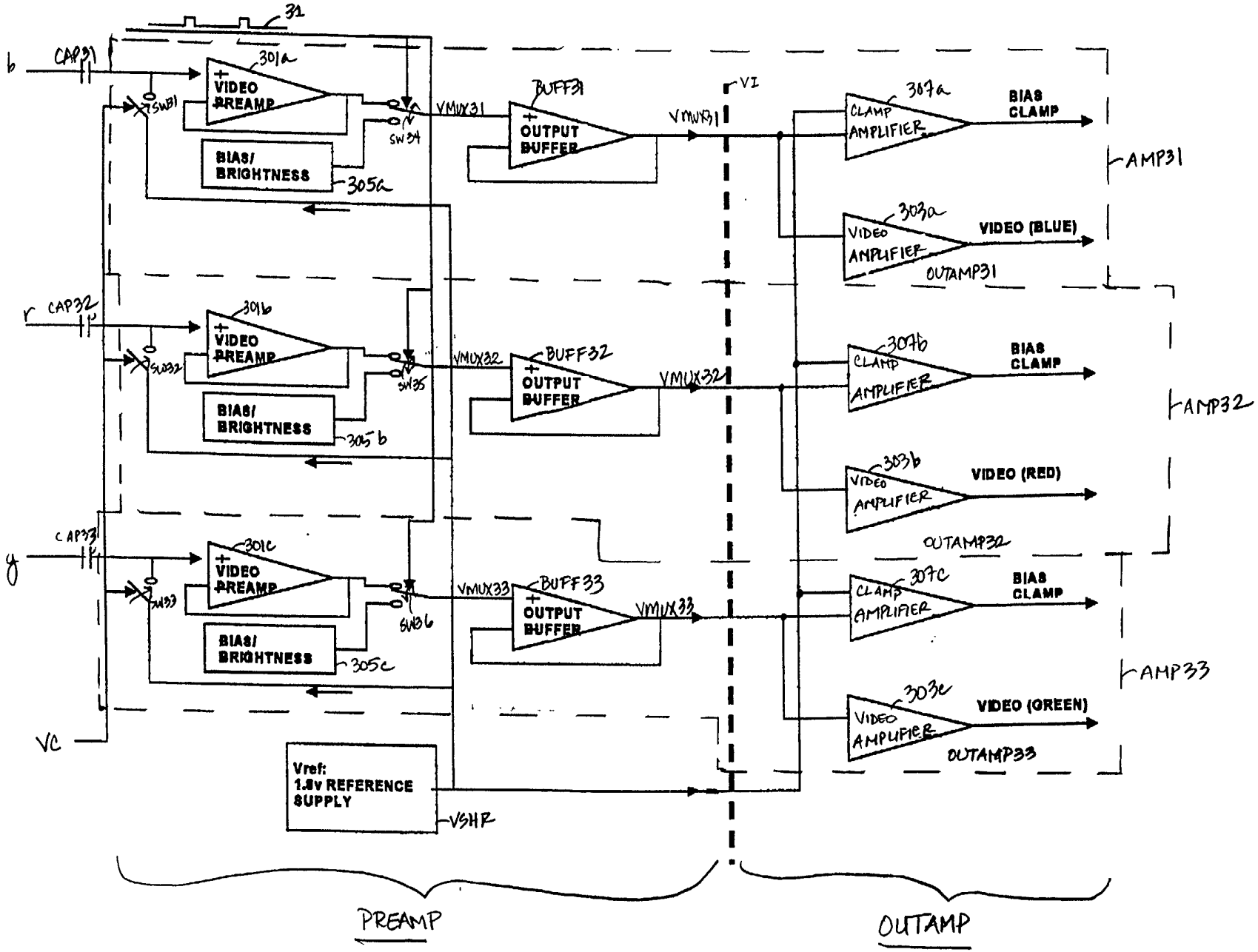
32
b
CAP31
301a
VIDEO PREAMP
SW31
SW34
VMUX31
BUFF31
OUTPUT BUFFER
VMUX31
VI
307a
CLAMP AMPLIFIER
BIAS CLAMP
AMP31
BIAS/ BRIGHTNESS
305a
303a
VIDEO AMPLIFIER
VIDEO (BLUE)
OUTAMP31
r
CAP32
301b
VIDEO PREAMP
SW32
SW35
VMUX32
BUFF32
OUTPUT BUFFER
VMUX32
307b
CLAMP AMPLIFIER
BIAS CLAMP
AMP32
BIAS/ BRIGHTNESS
305b
303b
VIDEO AMPLIFIER
VIDEO (RED)
OUTAMP32
g
CAP33
301c
VIDEO PREAMP
SW33
SW36
VMUX33
BUFF33
OUTPUT BUFFER
VMUX33
307c
CLAMP AMPLIFIER
BIAS CLAMP
AMP33
BIAS/ BRIGHTNESS
305c
303c
VIDEO AMPLIFIER
VIDEO (GREEN)
OUTAMP33
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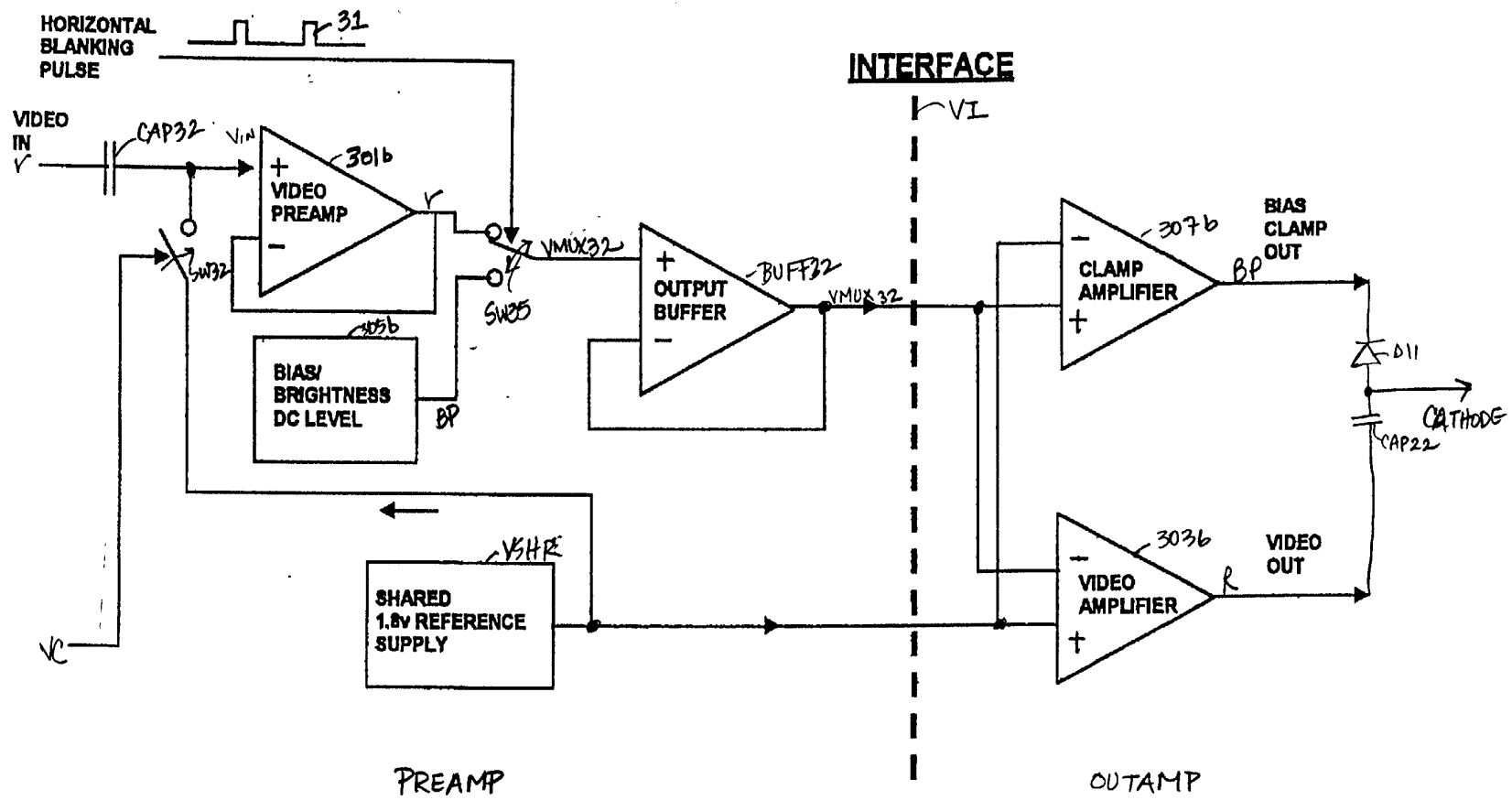
Vref: 1.8v REFERENCE SUPPLY
VSHR
PREAMP
OUTAMP

300

FIGURE 6



AMP32

FIGURE 7

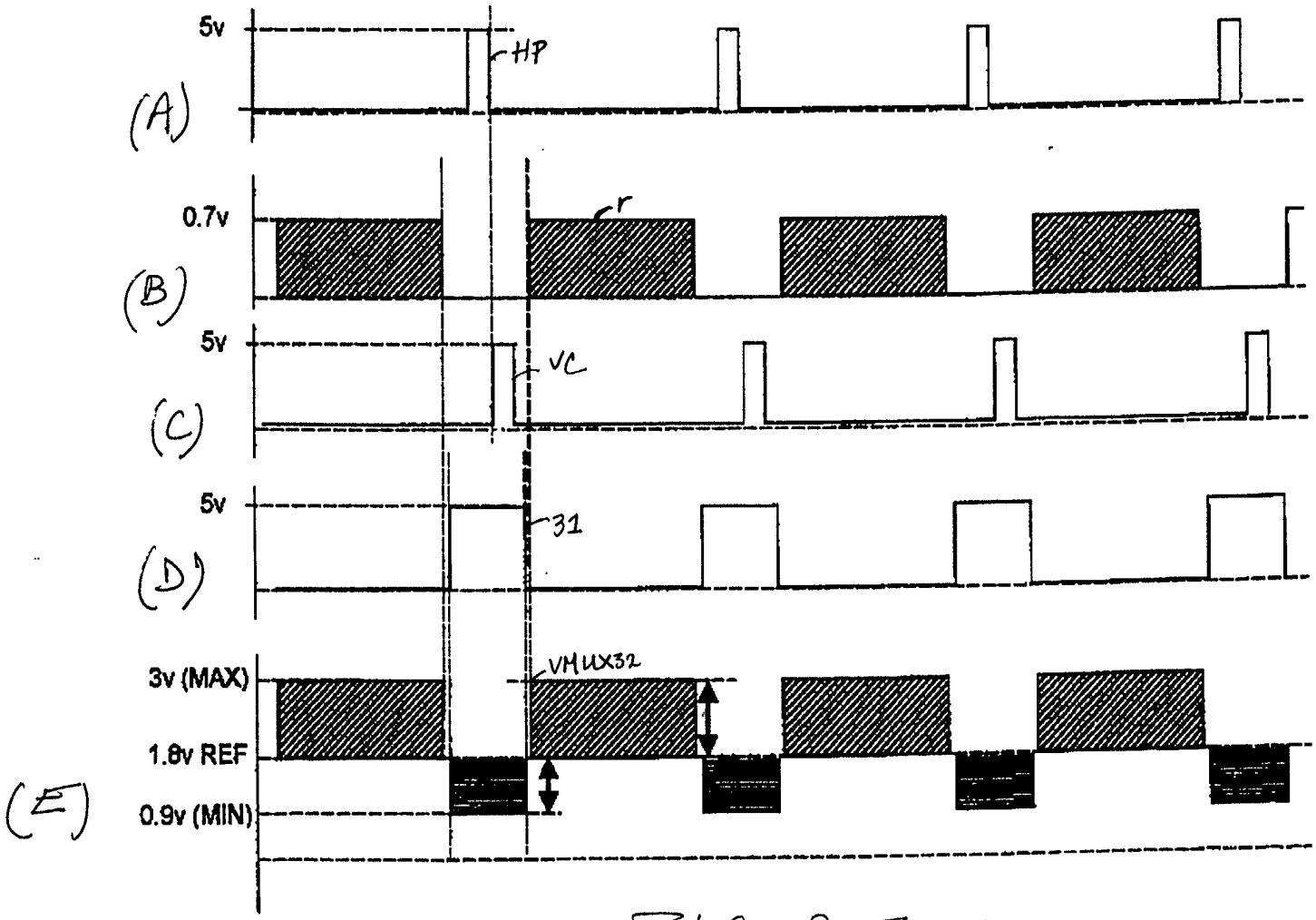


FIGURE 8

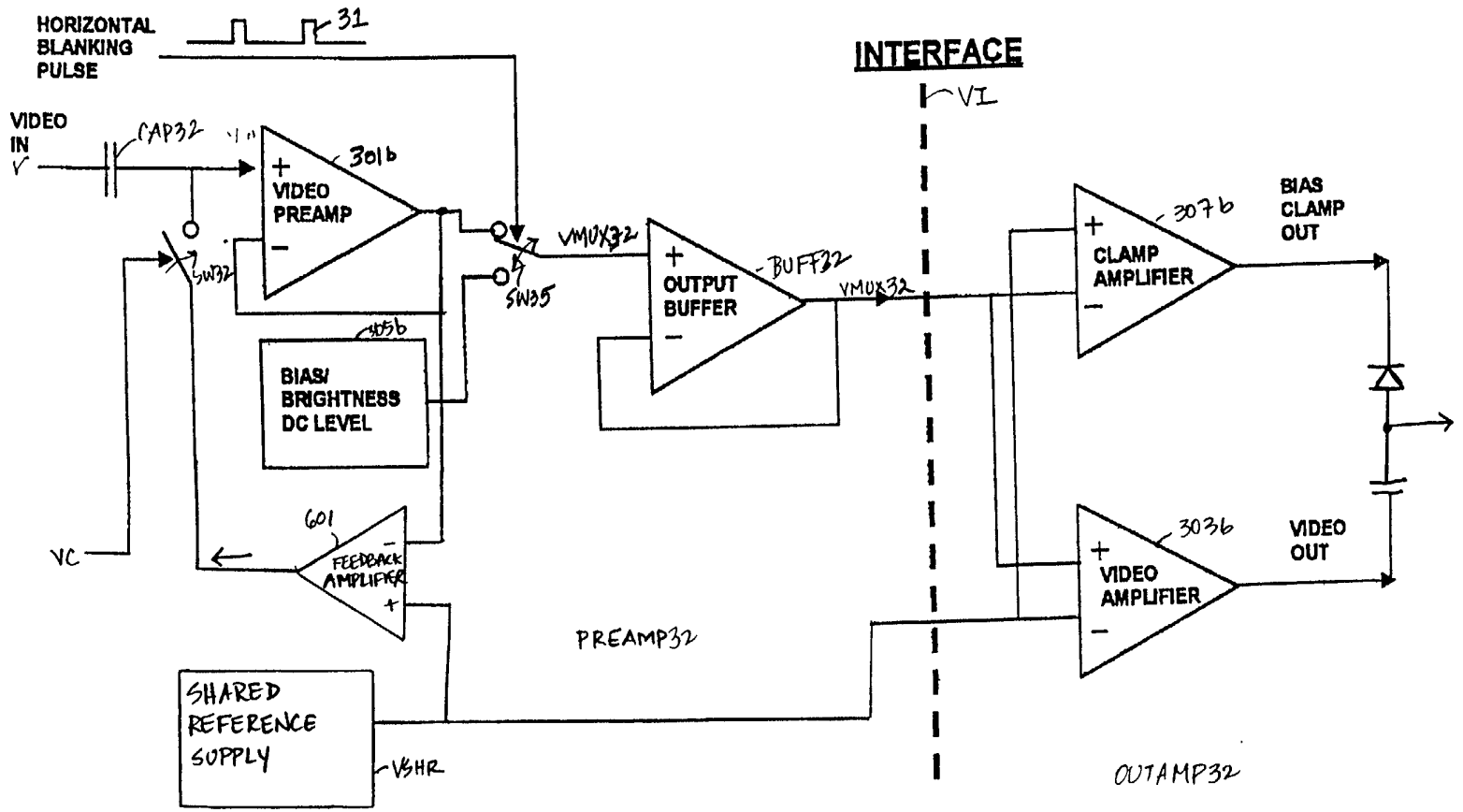

HORIZONTAL BLANKING PULSE
31
INTERFACE
VI
VIDEO IN
CAP32
301b
VIDEO PREAMP
SW32
SW35
VMUX32
BUFF32
OUTPUT BUFFER
VMUX32
307b
CLAMP AMPLIFIER
BIAS CLAMP OUT
305b
BIAS/ BRIGHTNESS DC LEVEL
VC
601
FEEDBACK AMPLIFIER
PREAMP32
3036
VIDEO AMPLIFIER
VIDEO OUT
SHARED REFERENCE SUPPLY
VSHR
OUTAMP32

FIGURE 9

0.95 - 1.25 - 1.55 - 0.95 - 1.25 - 1.55

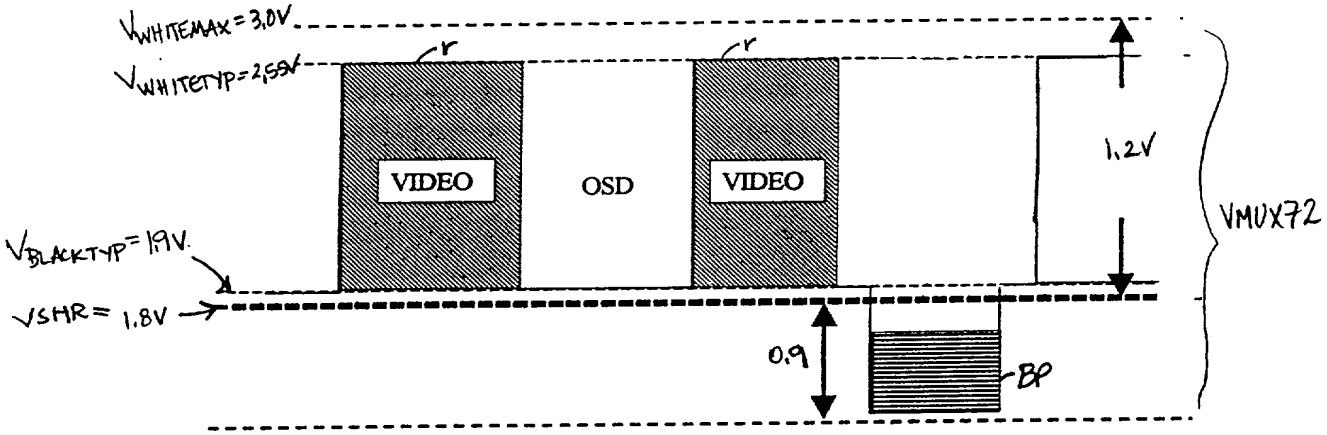


FIGURE 10

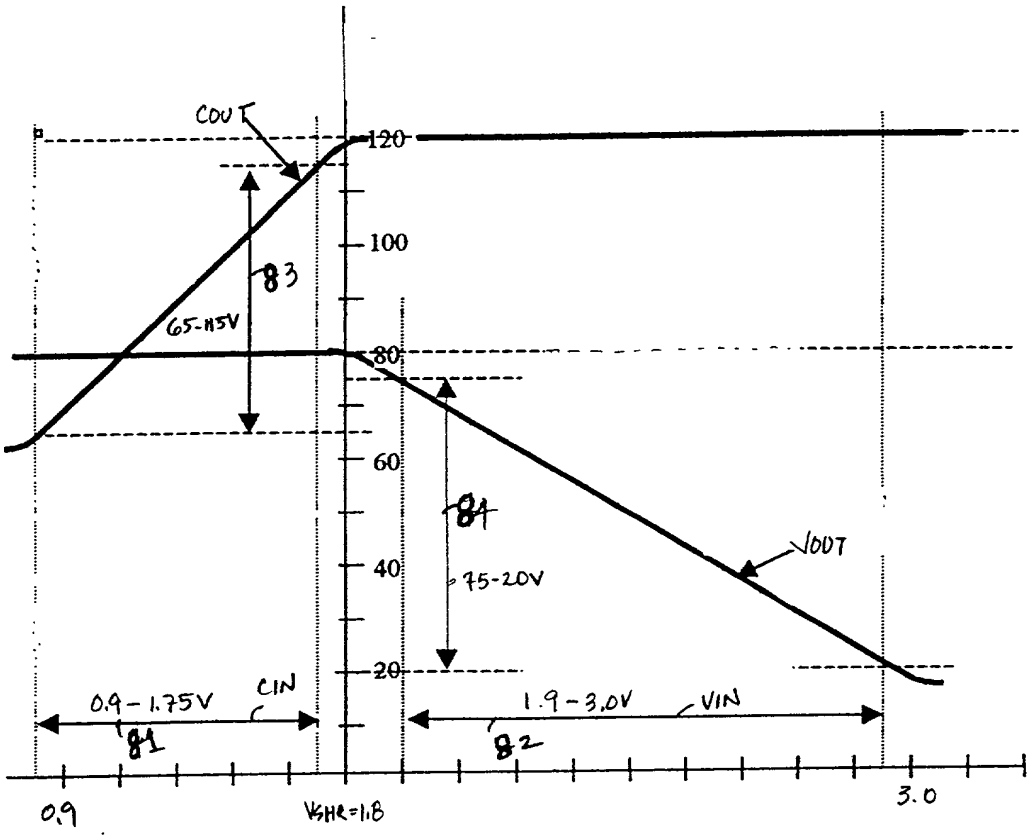


FIGURE 11

09/09/36 - 1027700

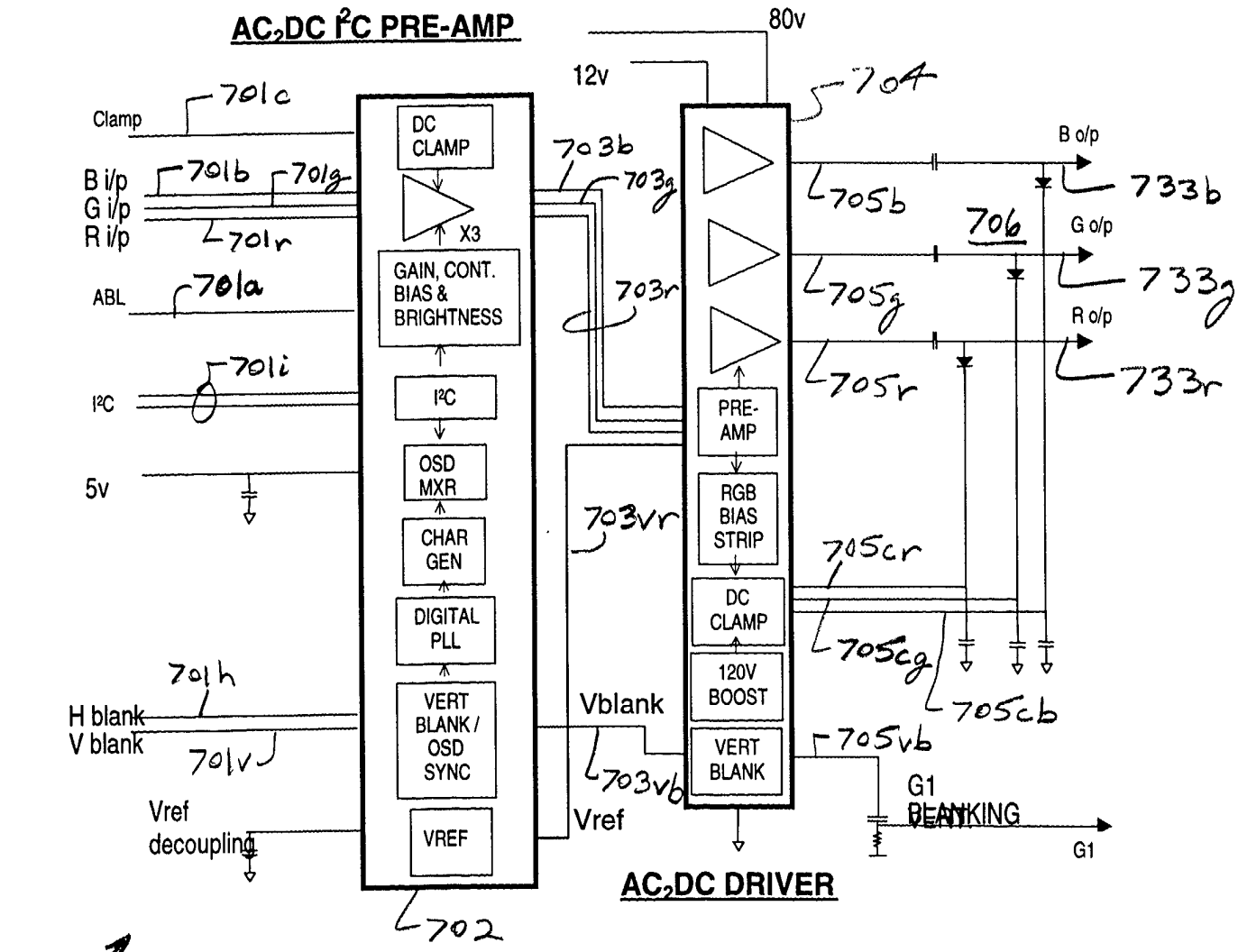

AC2DC I2C PRE-AMP
80v
12v
704
Clamp
701c
B i/p
G i/p
R i/p
701b
701g
701r
ABL
701a
I2C
701i
5v
DC CLAMP
X3
GAIN, CONT. BIAS & BRIGHTNESS
I2C
OSD MXR
CHAR GEN
DIGITAL PLL
VERT BLANK / OSD SYNC
VREF
703b
703g
703r
703vr
Vblank
703vb
Vref
PRE-AMP
RGB BIAS STRIP
DC CLAMP
120V BOOST
VERT BLANK
705b
705g
705r
705cr
705cg
705cb
705vb
706
B o/p
G o/p
R o/p
733b
733g
733r
G1 BLANKING
G1
701h
H blank
V blank
701v
Vref decoupling
AC2DC DRIVER
702
700

FIGURE 12

AMPAD 22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS

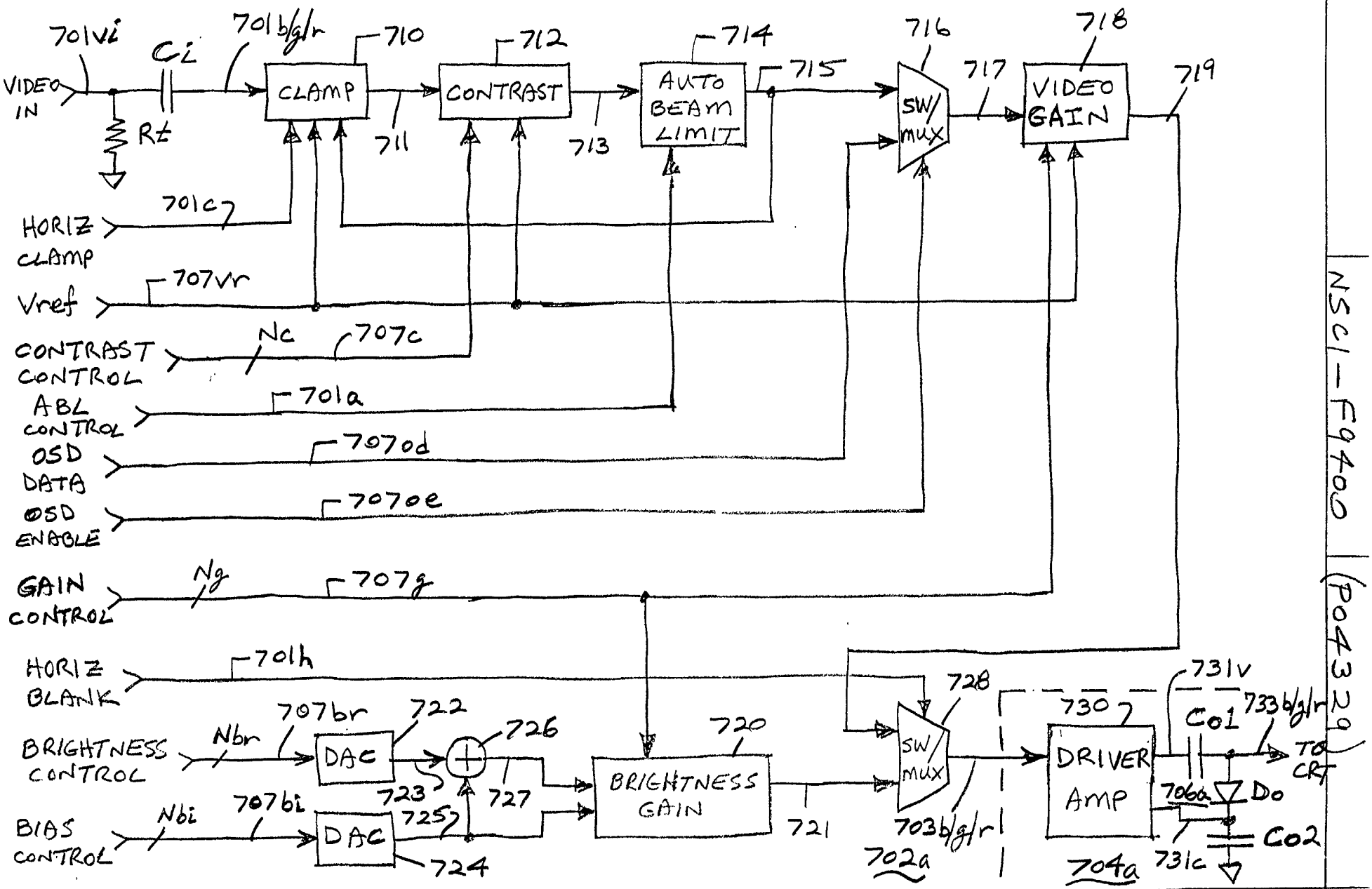


FIGURE 13

NSC1-F9400 (P043329)

National Semiconductor

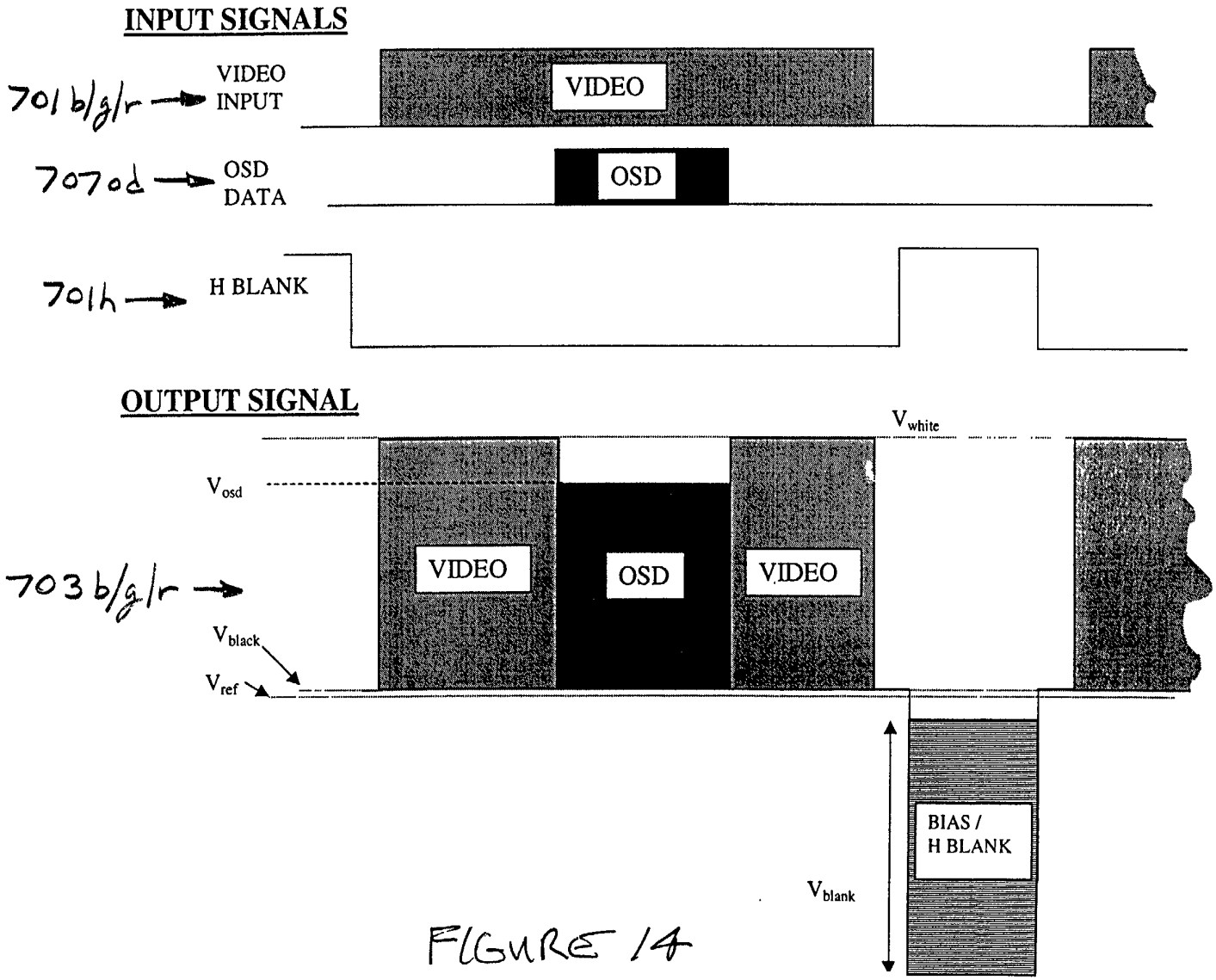


FIGURE 14

National Semiconductor

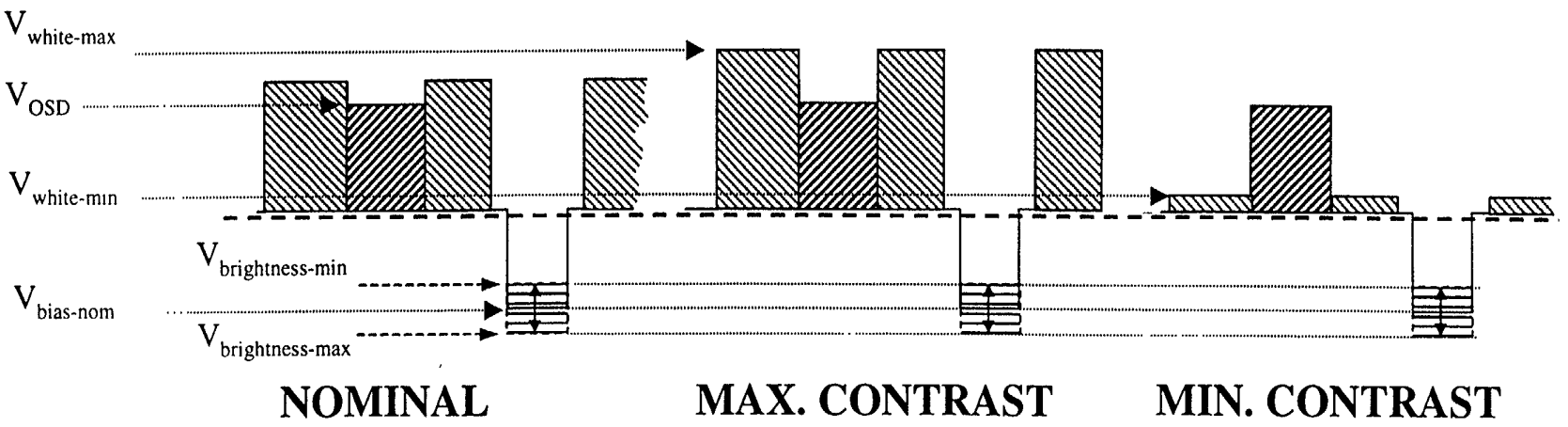


FIGURE 15

National Semiconductor

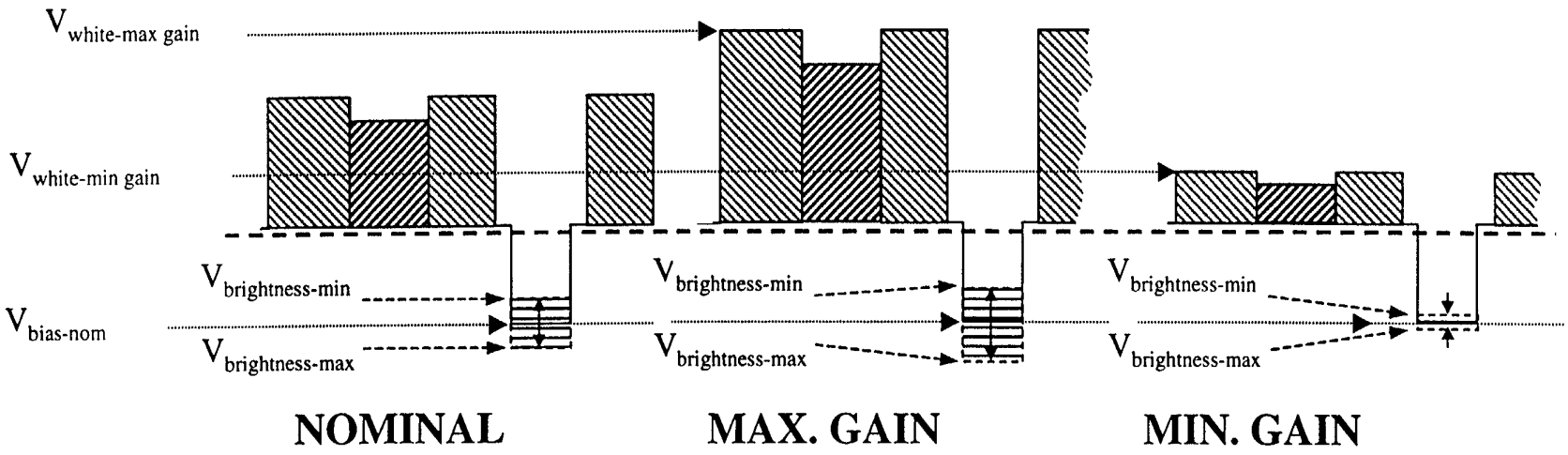


FIGURE 16

National Semiconductor

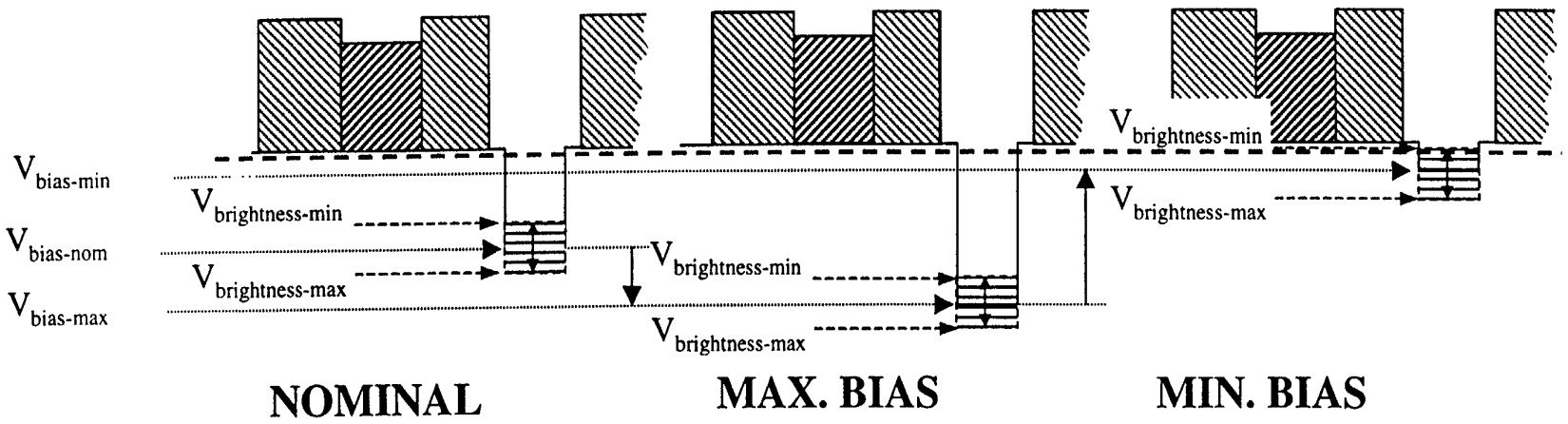
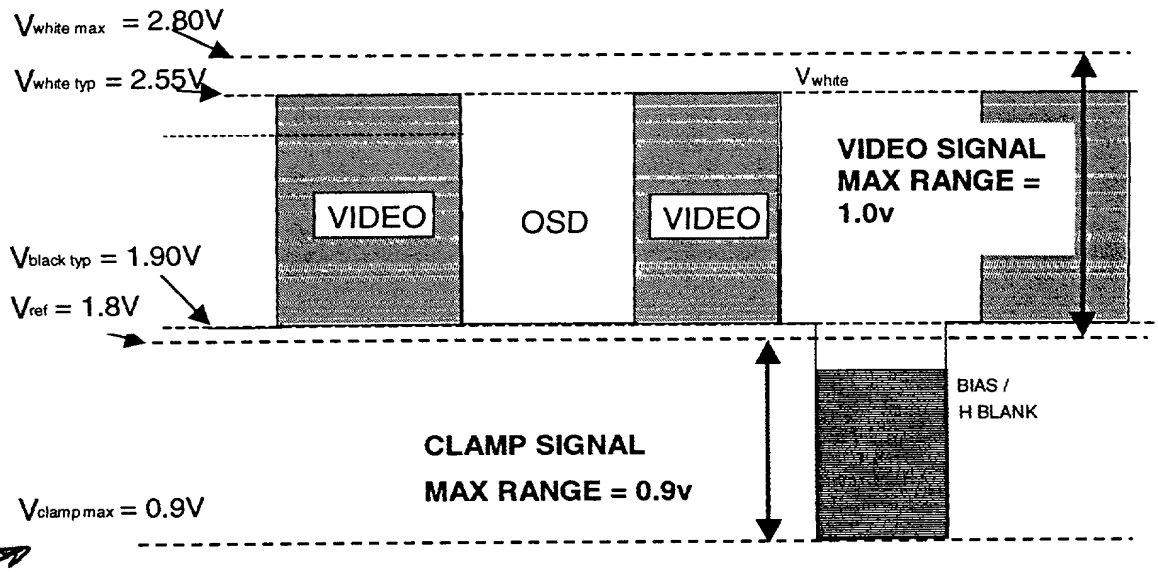


FIGURE 17



703 b/g/r

FIGURE 18

04/27/00 - H:\DOCS\SS\SS703.DOC

AMPAD 22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS
DO-20T "GE/86960"

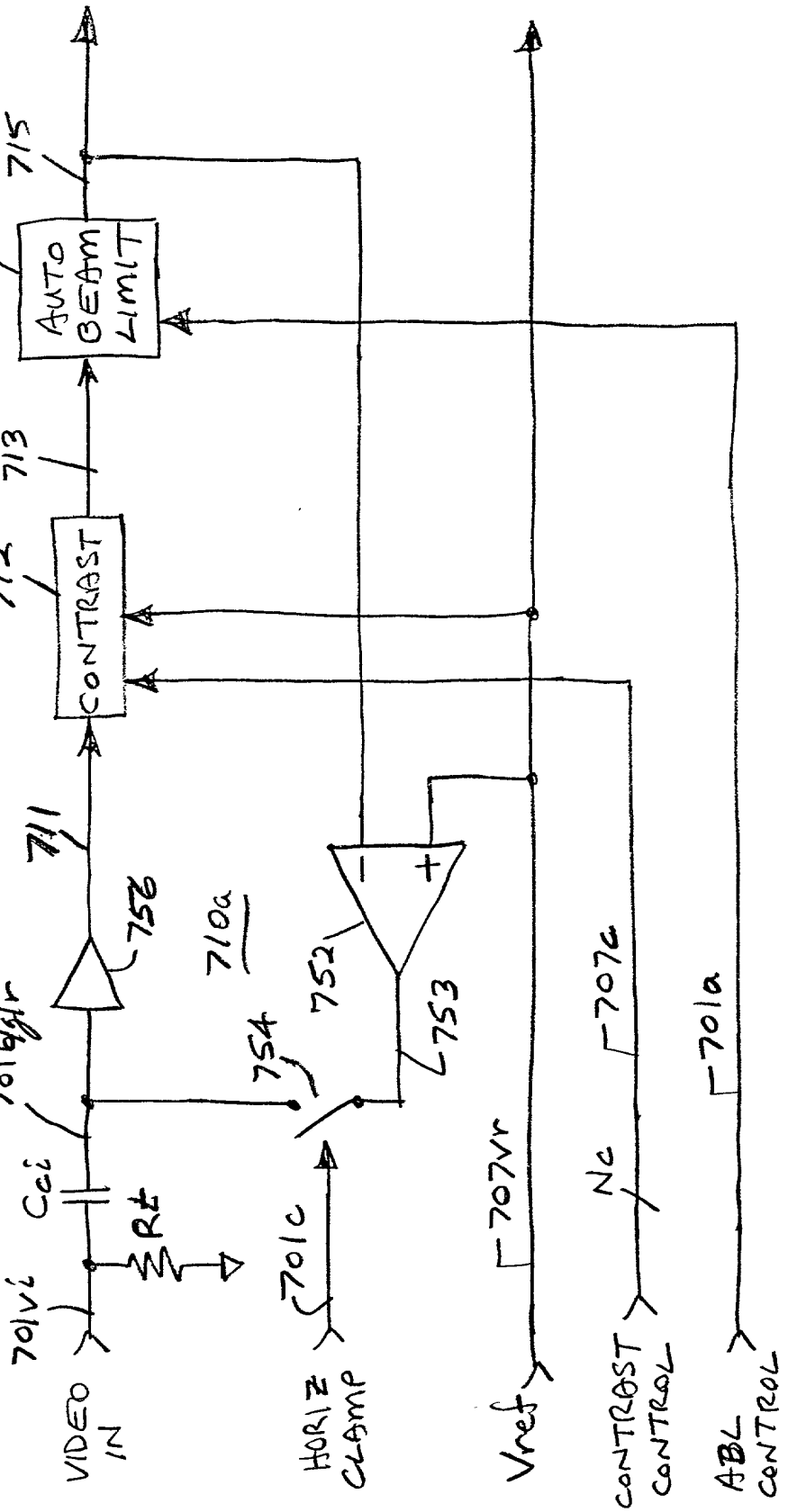


FIGURE 19

00/201"6E/86960

AMPAD 22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS

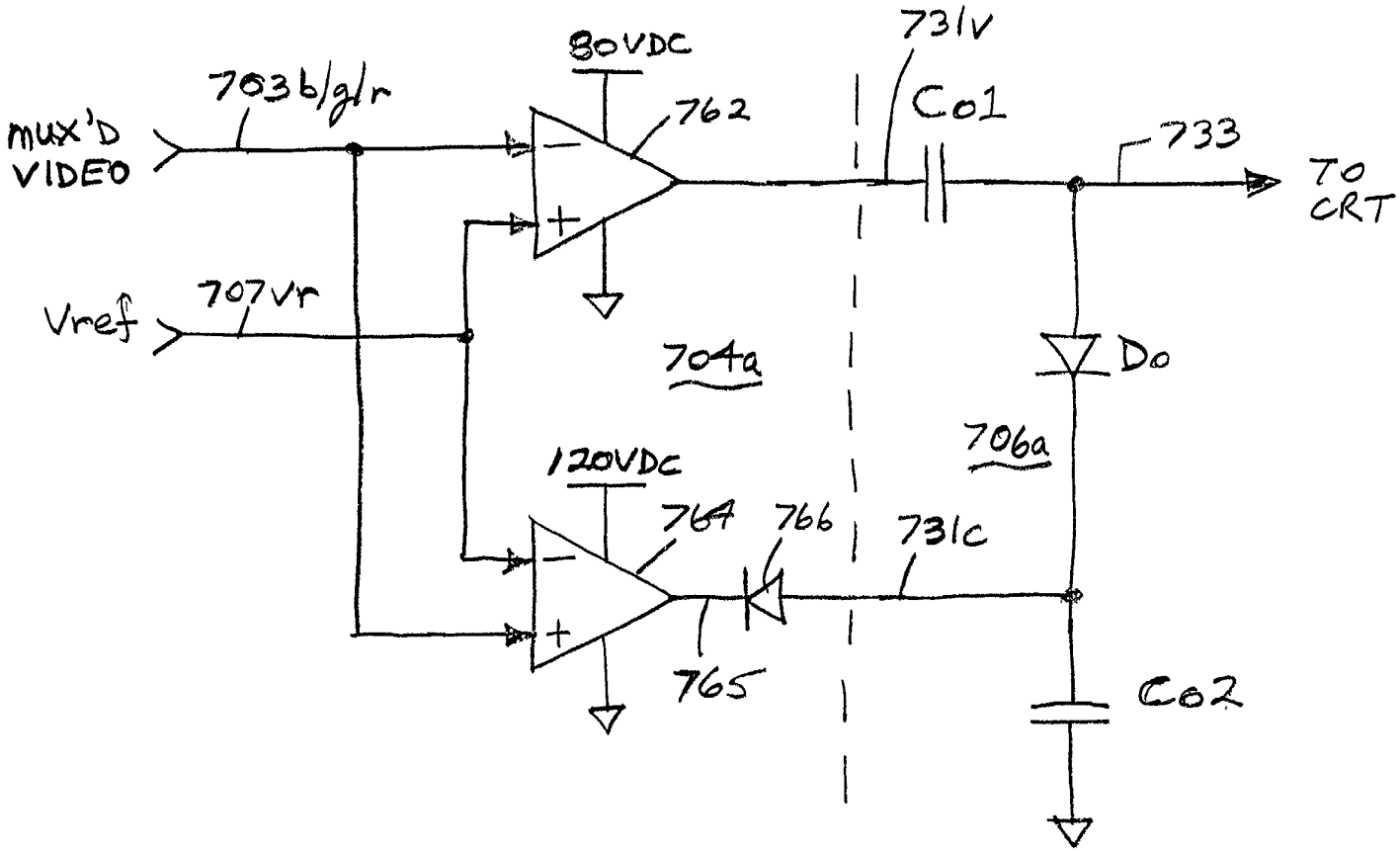
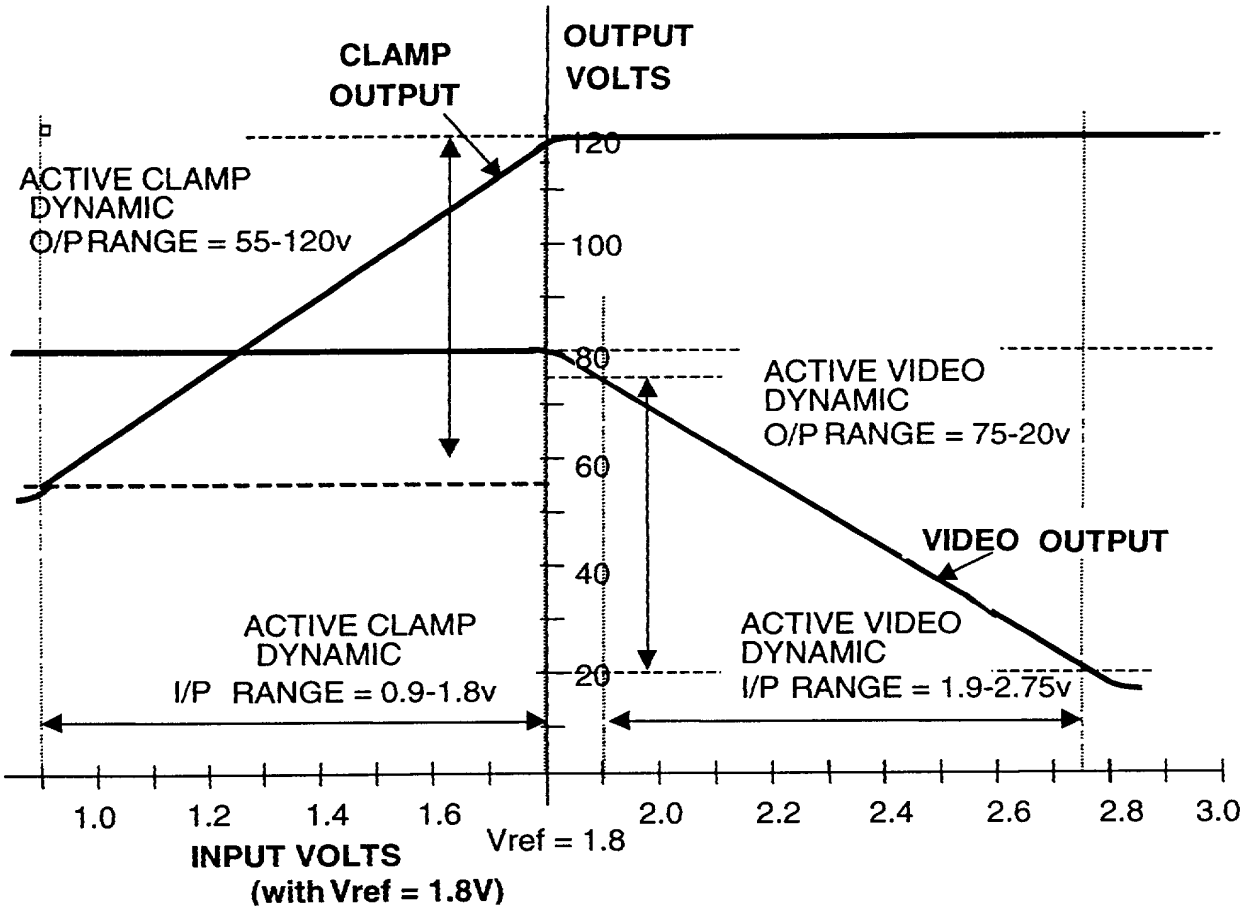


FIGURE 20

NSCI-F9400 (P04329)



(Test Conditions: V_{ref} = 1.8v, Vcc1 = 80v, Vcc2 = 120v, Vbb = 12v)

FIGURE 21

0047201 "SE/8850

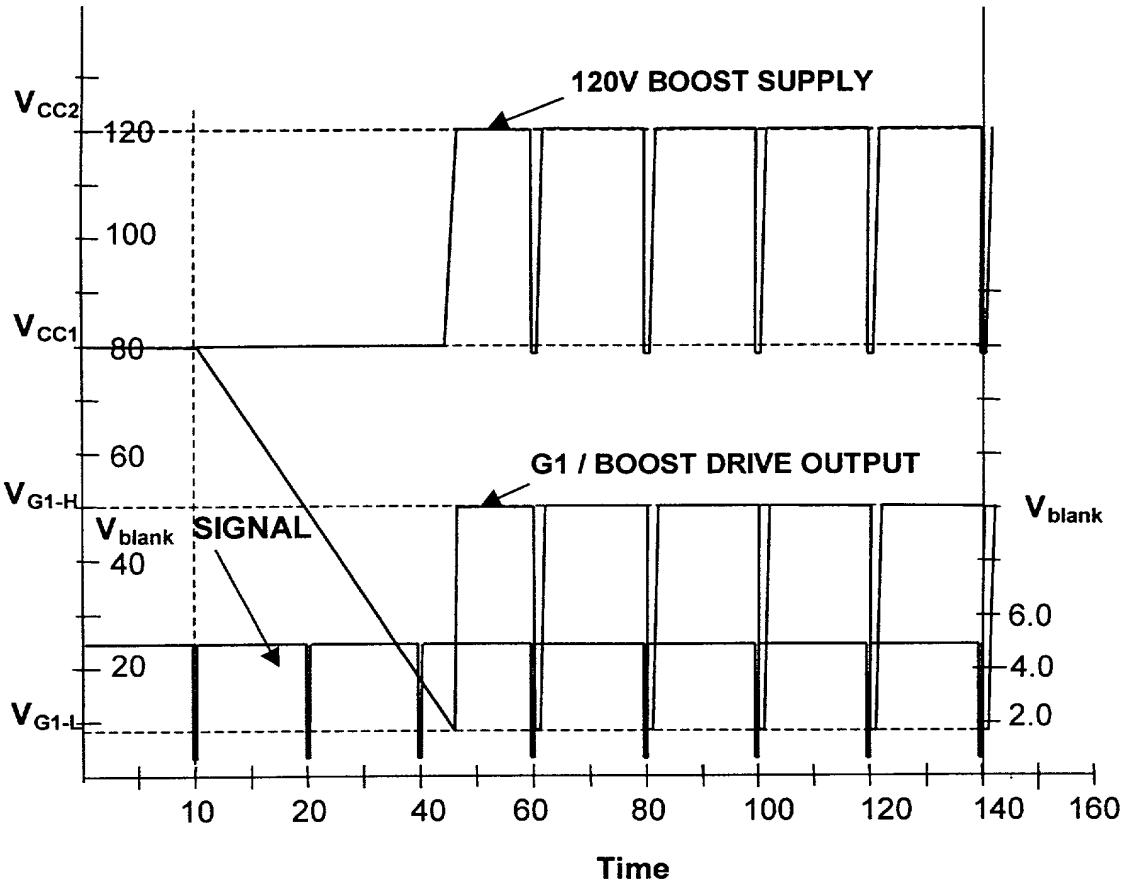

120V BOOST SUPPLY
V_{CC2}
120
100
V_{CC1}
80
60
G1 / BOOST DRIVE OUTPUT
V_{G1-H}
V_{blank}
SIGNAL
40
20
V_{G1-L}
V_{blank}
6.0
4.0
2.0
10
20
40
60
80
100
120
140
160
Time

FIGURE 22

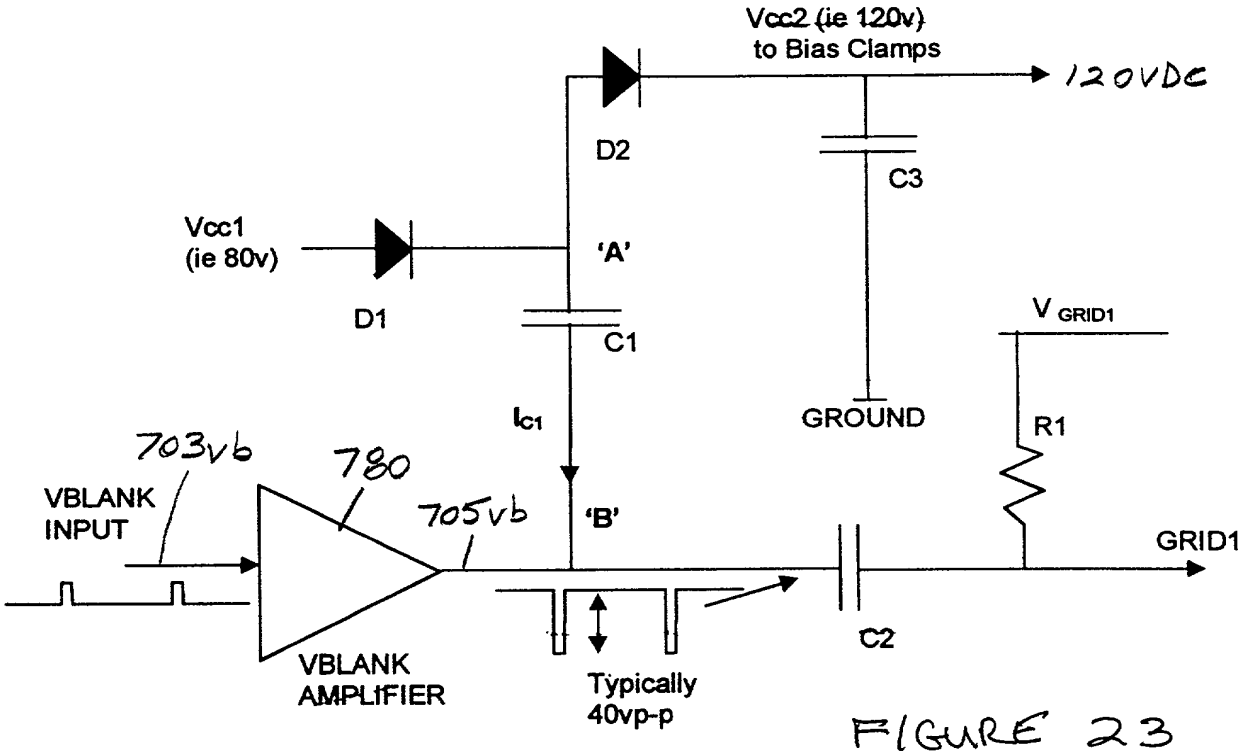


FIGURE 23

00/2207 * 05/05/00

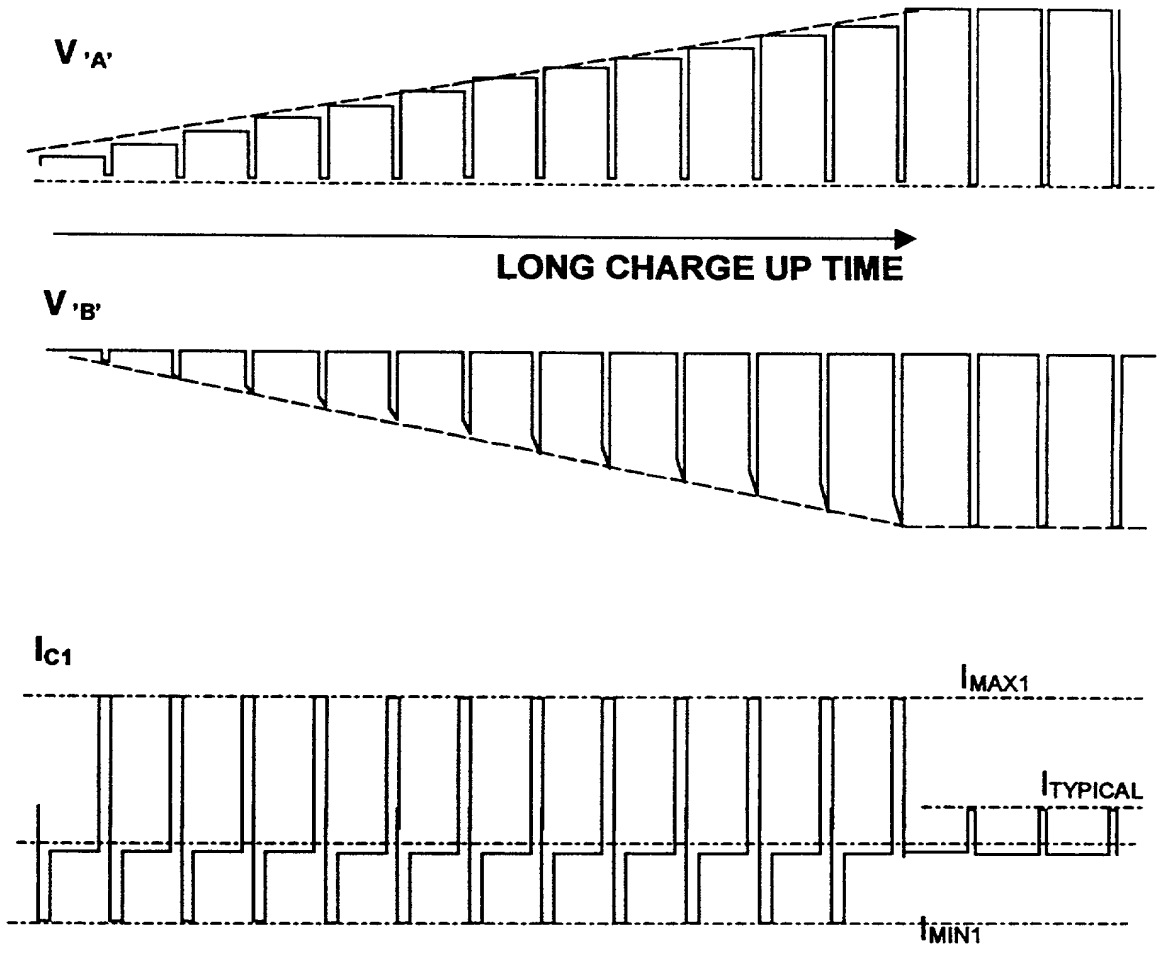


FIGURE 24

00/2017 - 95/85,669

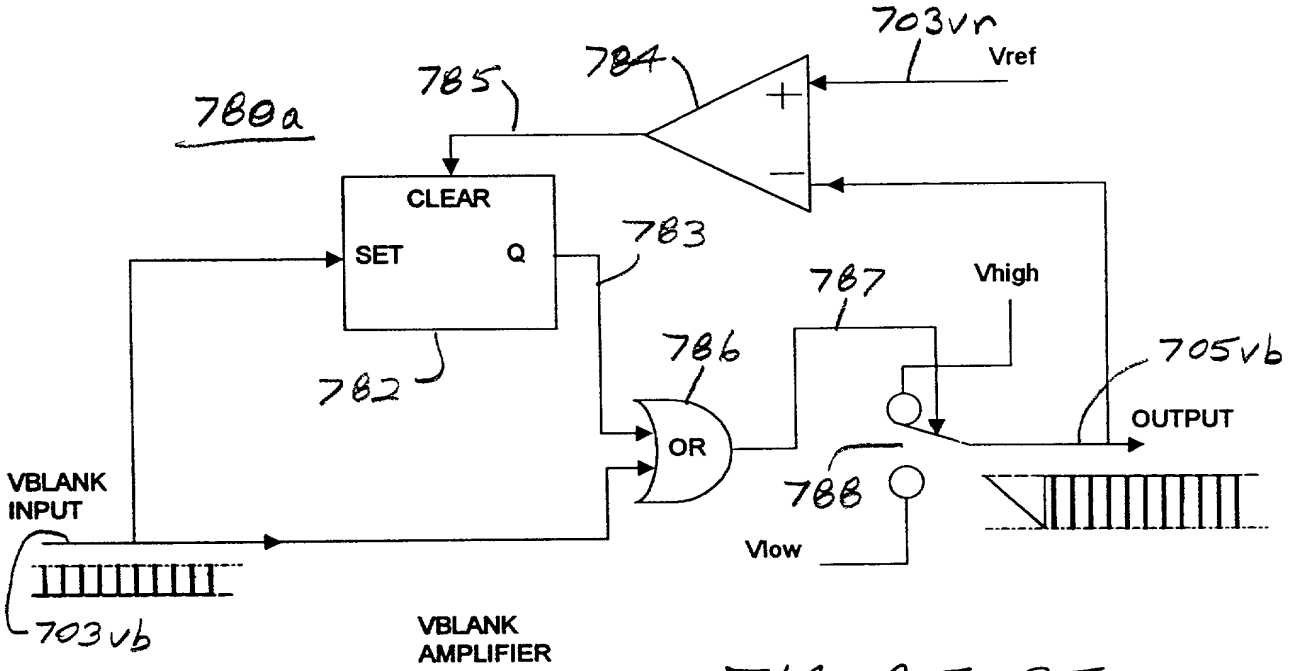


FIGURE 25

09/98/7E/2007

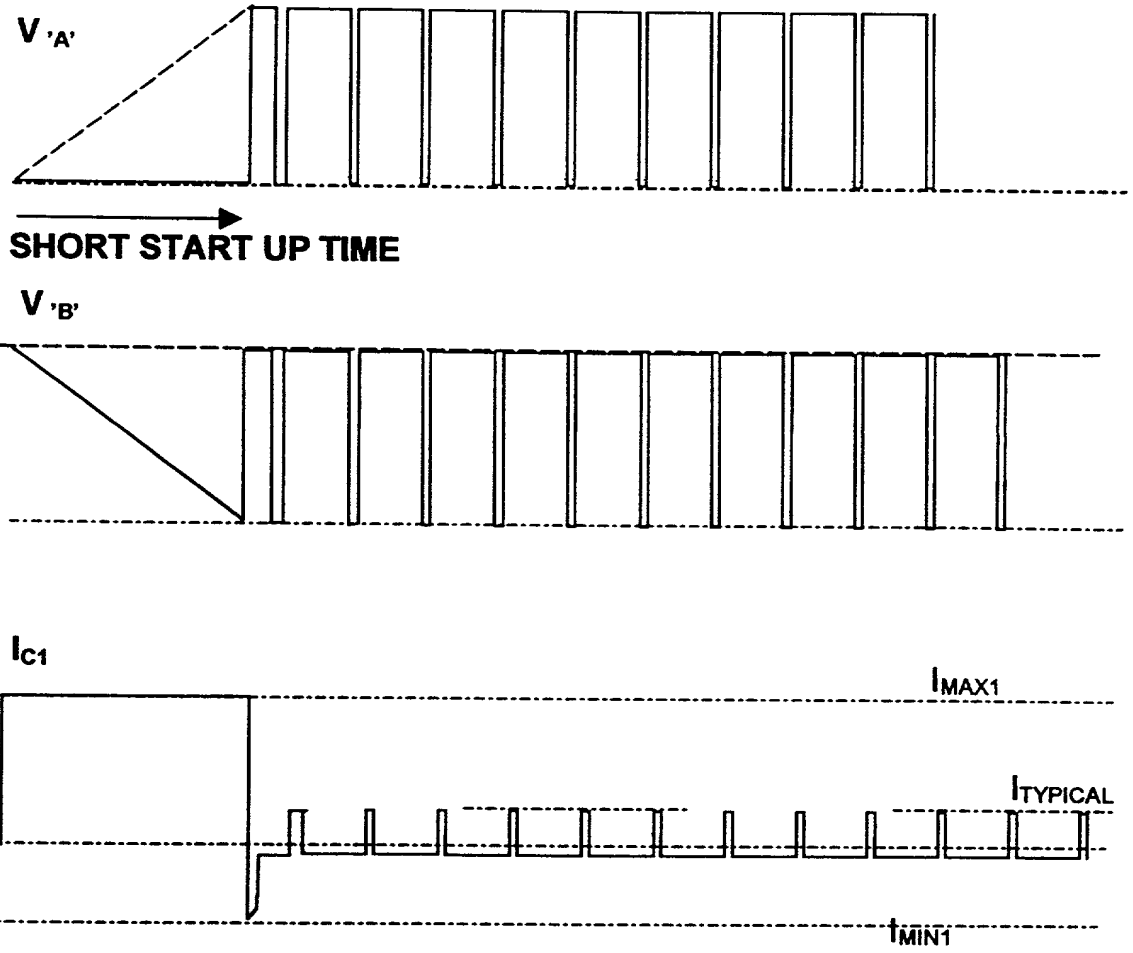


FIGURE 26

00/201 "6E/86960

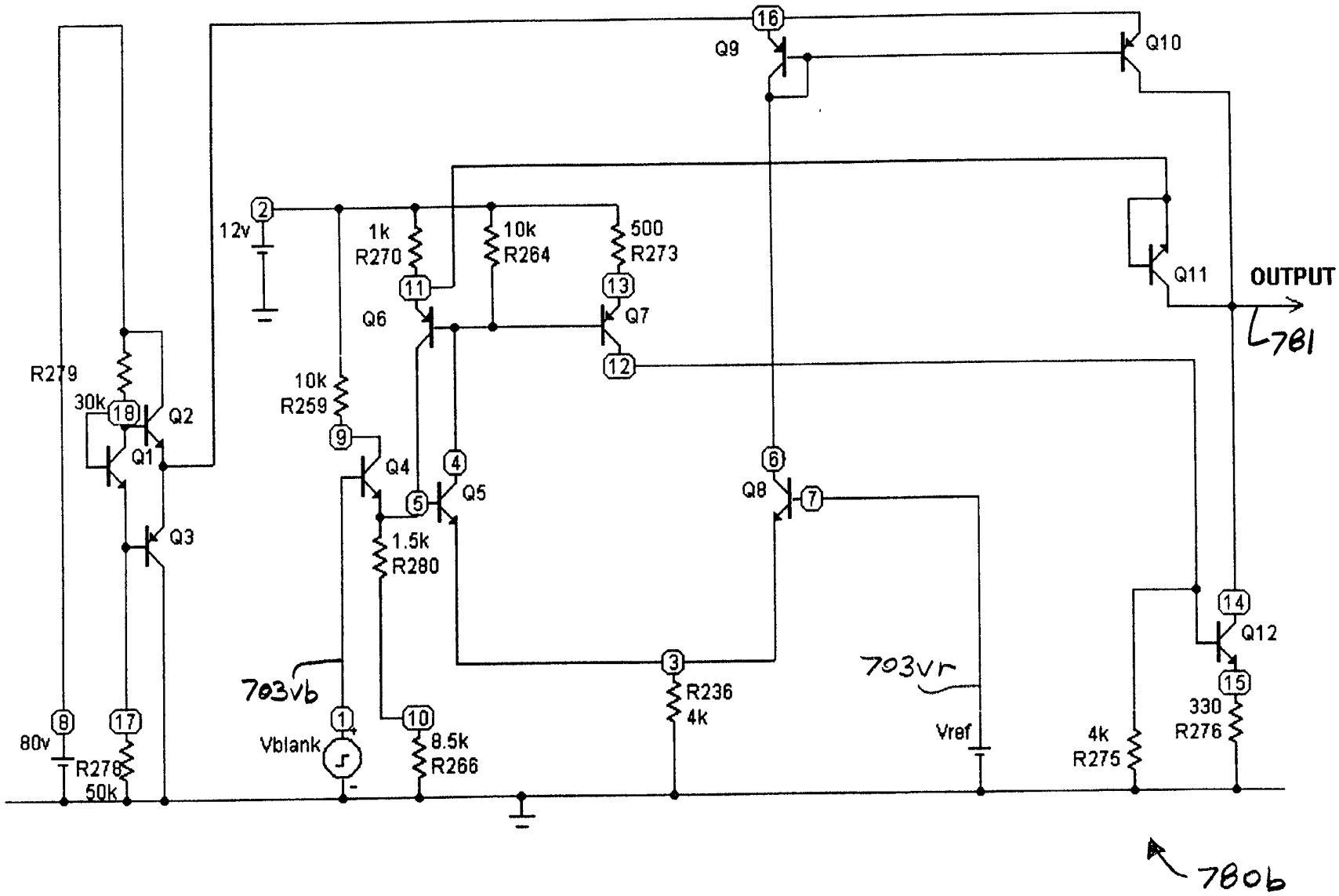


FIGURE 27

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD
00720T "6E/86960

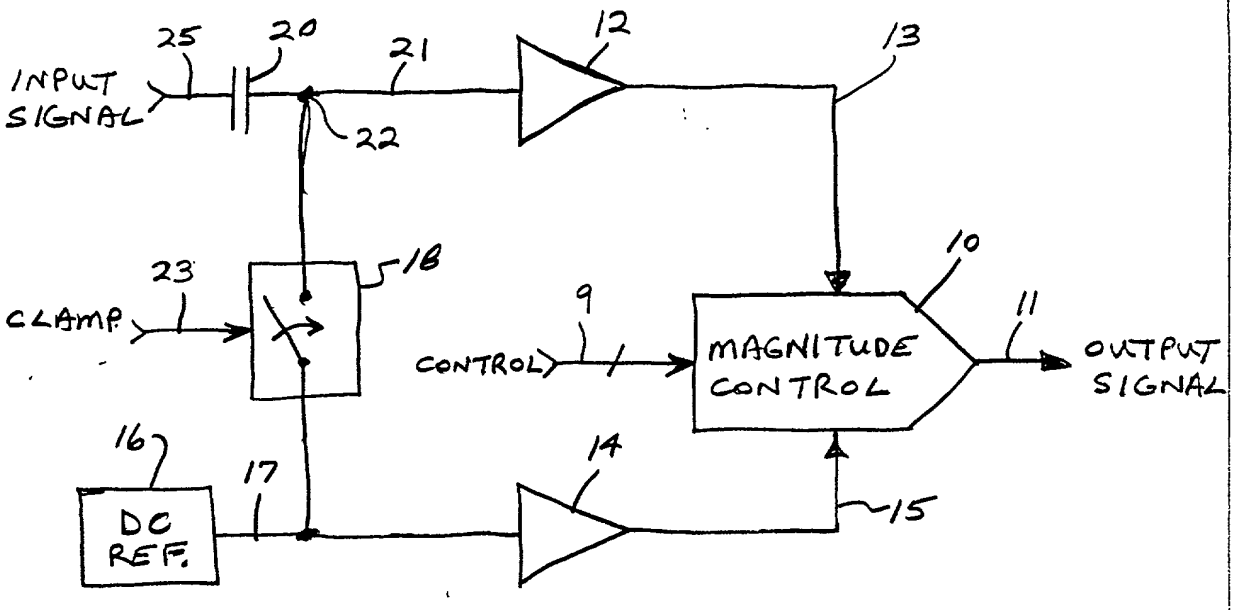


FIGURE 28

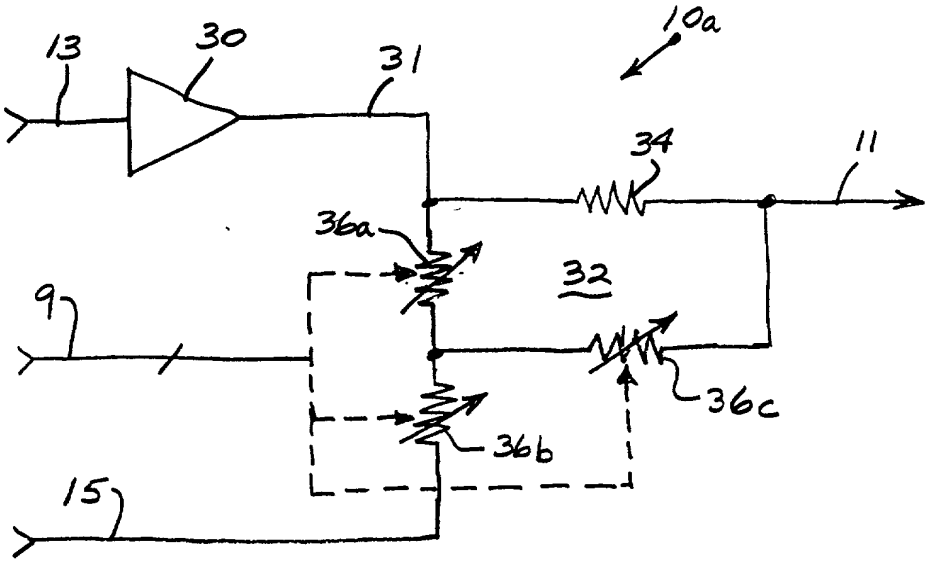


FIGURE 29

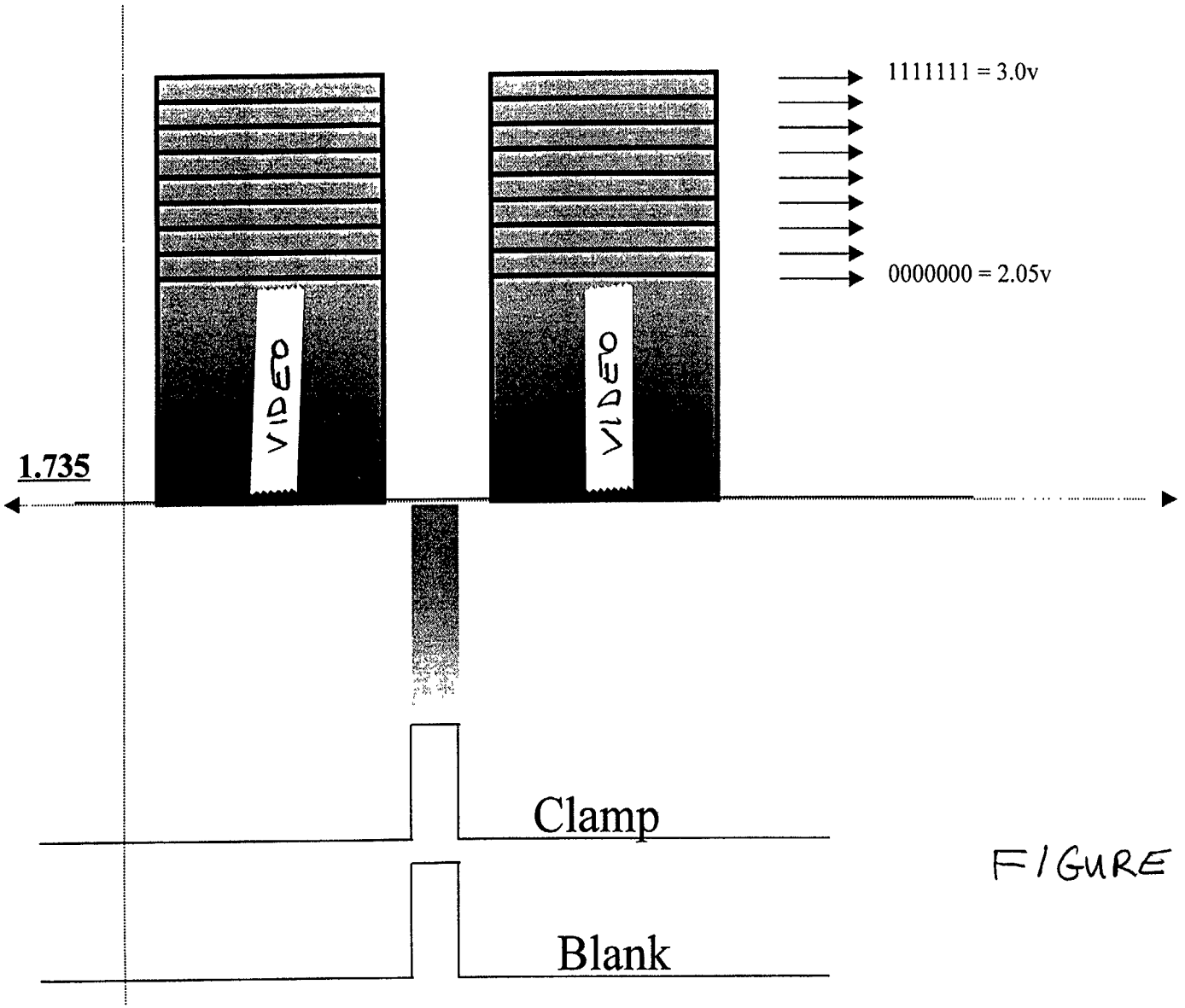


FIGURE 30

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

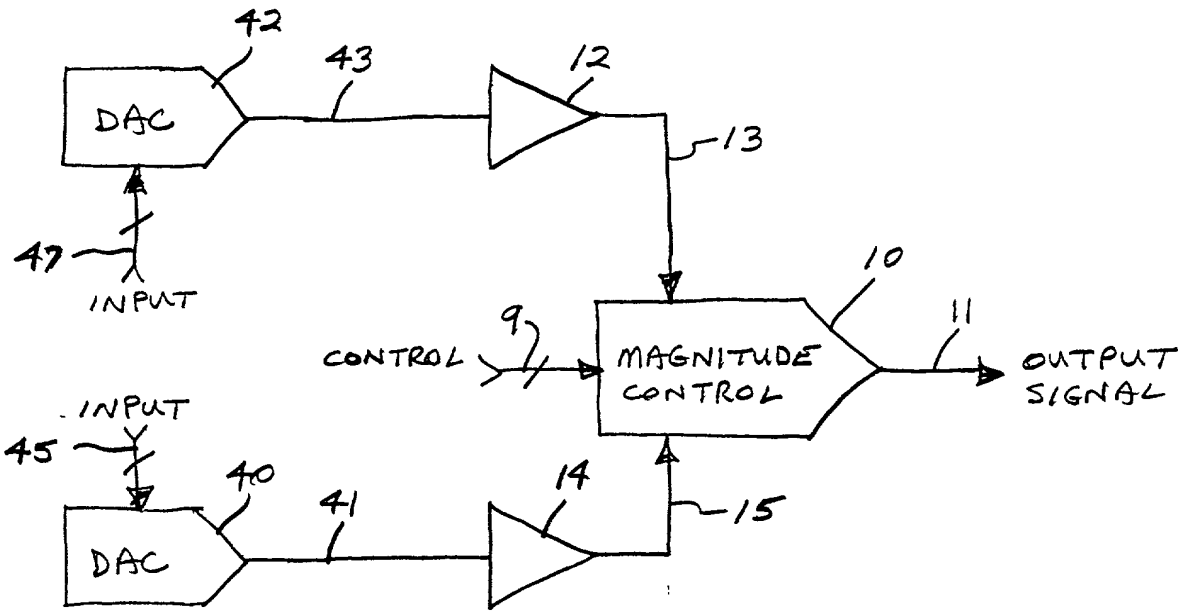


FIGURE 31

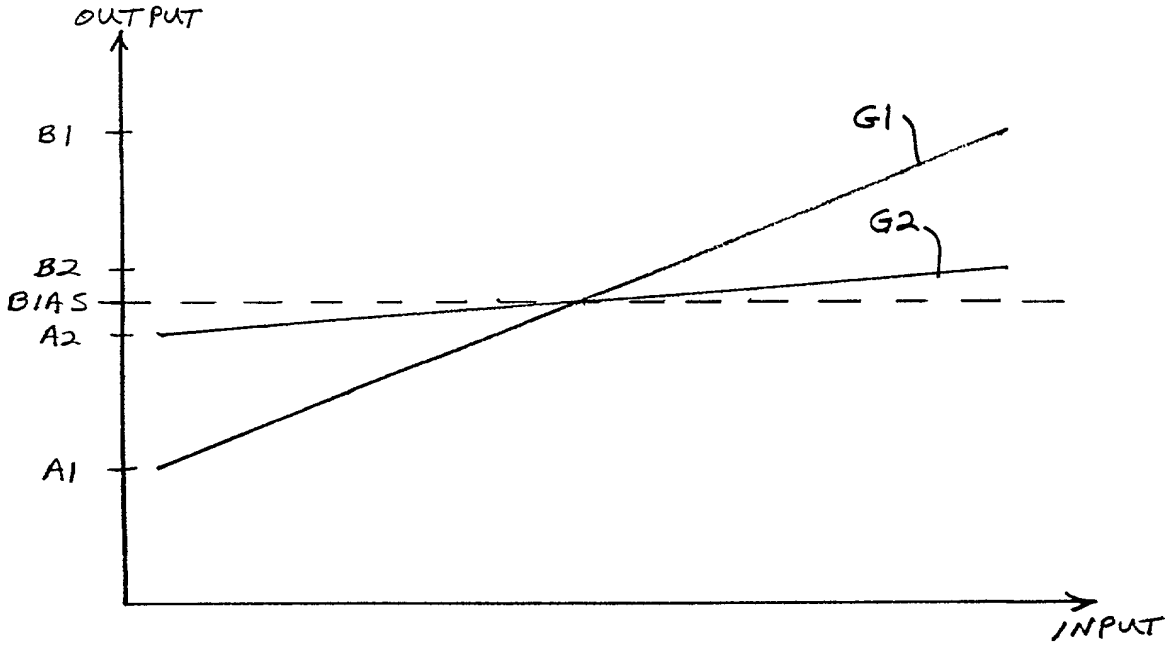


FIGURE 32

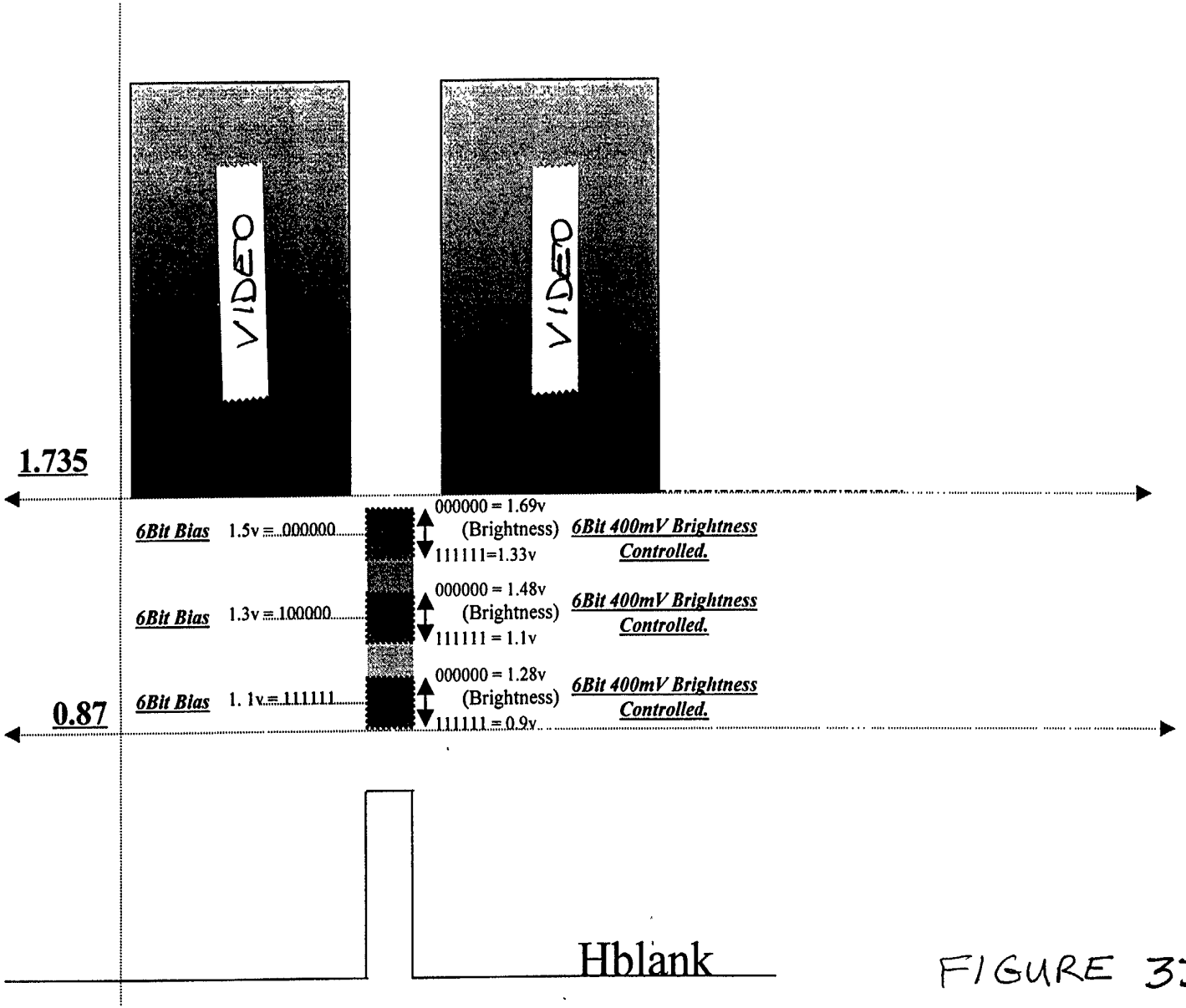

VIDEO
VIDEO
1.735
6Bit Bias
1.5v = 000000
000000 = 1.69v
(Brightness)
111111=1.33v
6Bit 400mV Brightness Controlled.
6Bit Bias
1.3v = 100000
000000 = 1.48v
(Brightness)
111111 = 1.1v
6Bit 400mV Brightness Controlled.
6Bit Bias
1. 1v = 111111
000000 = 1.28v
(Brightness)
111111 = 0.9v
6Bit 400mV Brightness Controlled.
0.87
Hblank

FIGURE 33

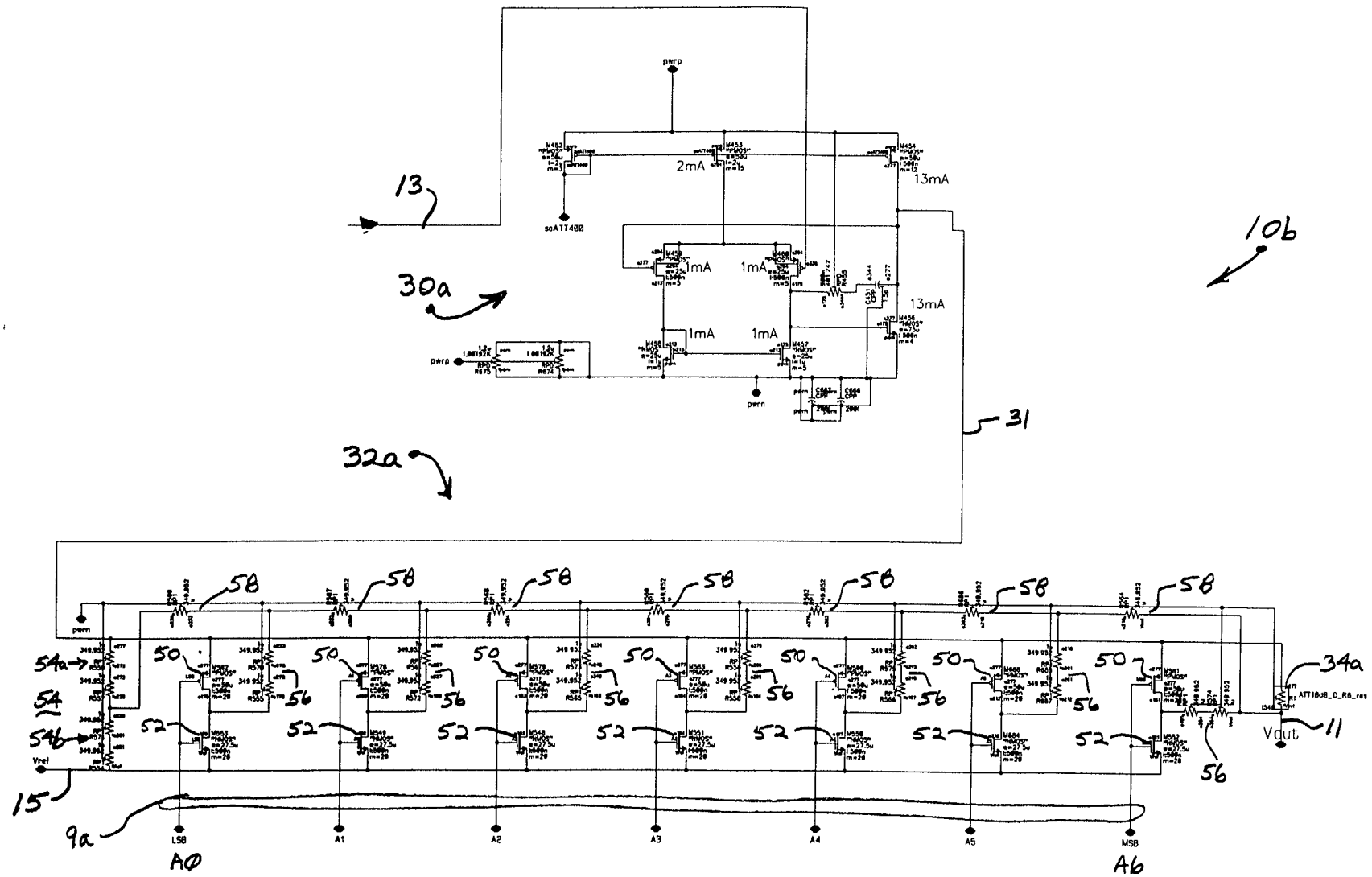

13
10b
30a
32a
31
2mA
13mA
1mA
1mA
1mA
1mA
13mA
pwrp
pwrn
soATT4dB
58
50
52
54
54a
54b
56
34a
Vout
11
Vref
15
9a
LSB
MSB
A0
A1
A2
A3
A4
A5
A6

FIGURE 34

09698739 "102700

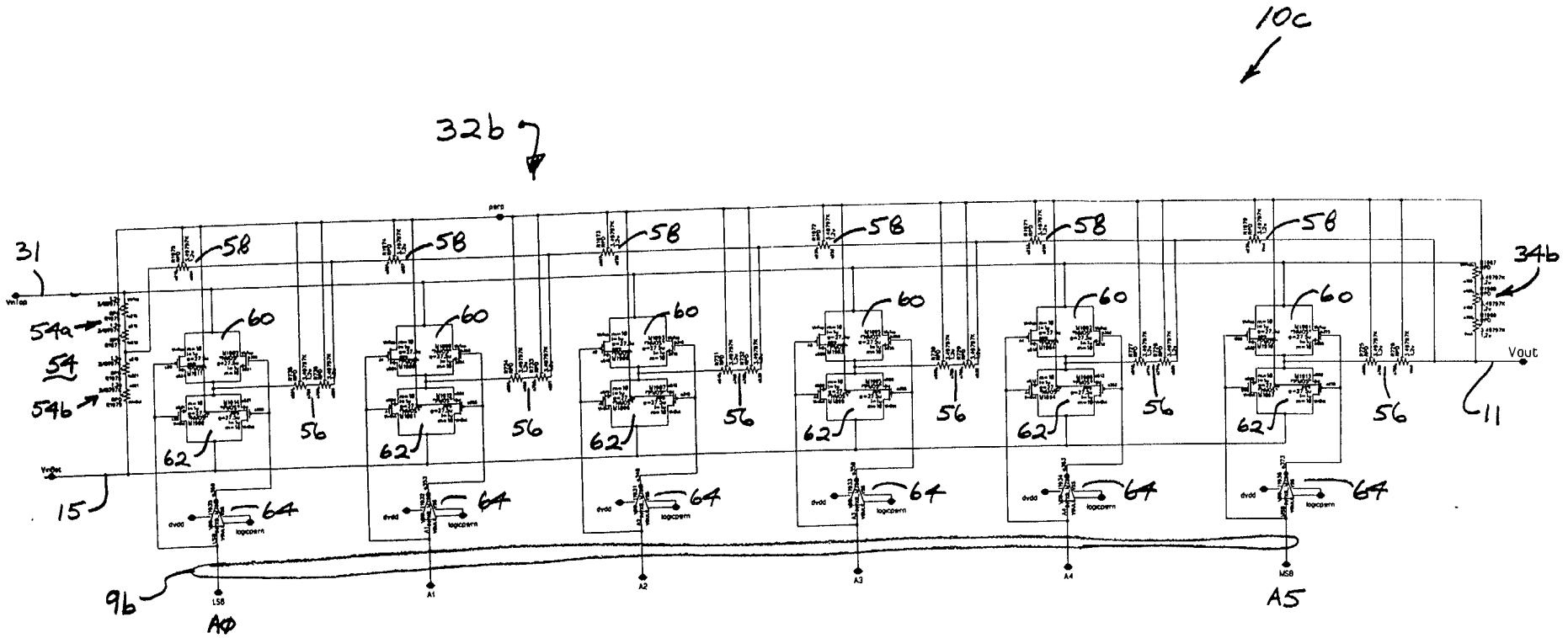


FIGURE 35

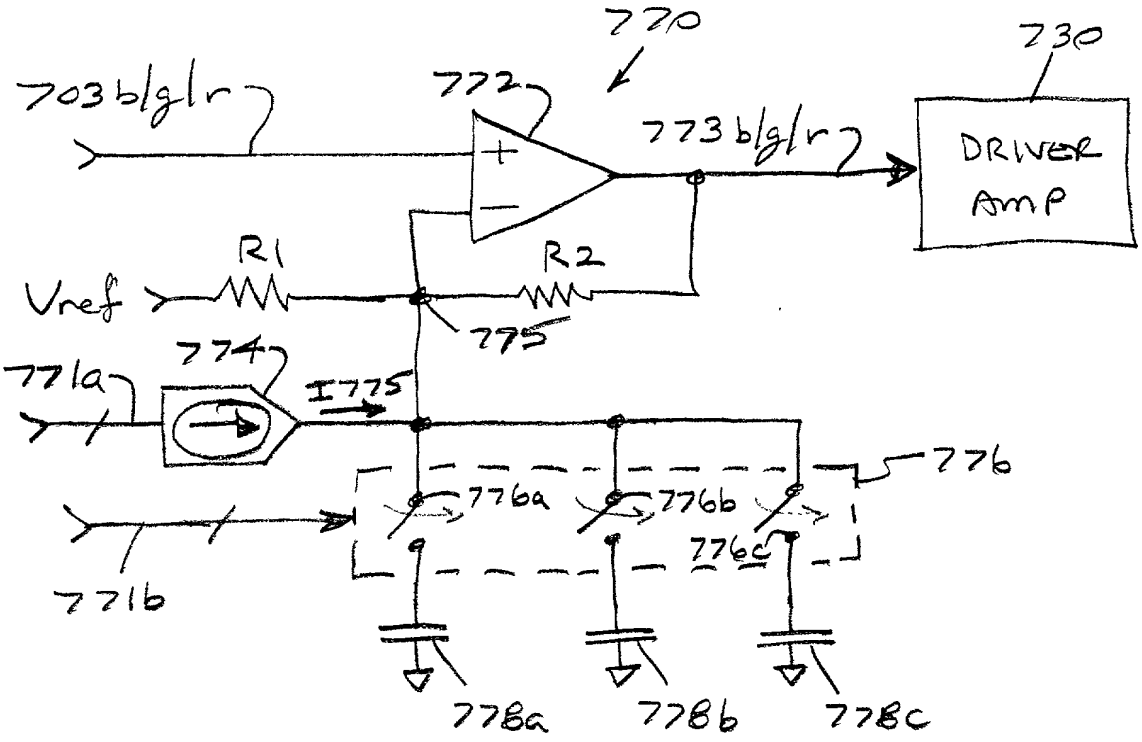


FIGURE 36

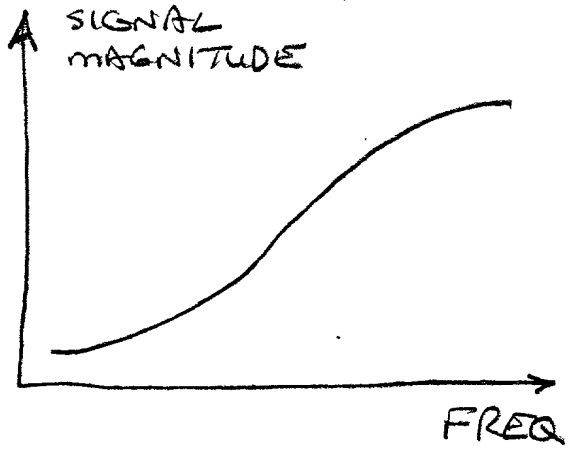


FIGURE 37

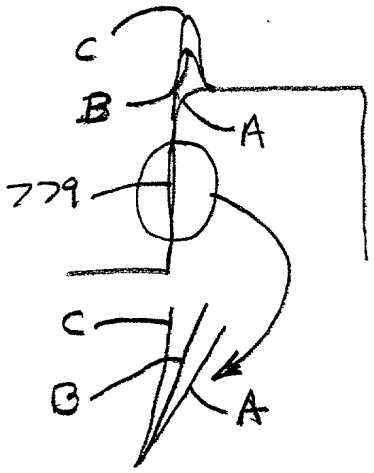


FIGURE 38

09659734 - 102704

EXPRESS MAIL NO.: EL563098702US

PATENT
Atty Docket No. 68135469-205220 [P04329 P01]

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MULTIPLEXED VIDEO SIGNAL INTERFACE SIGNAL, SYSTEM AND METHOD

the specification of which (check one) _X_ is attached hereto or __ was filed on ___ as Application No. __ and was amended on ___ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

60/153,013	09/09/00
Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

09/602,175	06/22/00	Pending
Application Number	Filing Date	Status: Patented, Pending, Abandoned
Application Number	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: PEYMAN HOJABRI

Inventor's signature _____ Date 10-23-00

Residence 967 Hampswood Way, San Jose, CA 95120

Citizenship U.S.A.

Post Office Address 967 Hampswood Way, San Jose, CA 95120

10/27/00 - 10:27 AM

EXPRESS MAIL NO.: EL563098702US

APPENDIX A

09696736 - 102700

LM2453
PRODUCT REQUIREMENT SPECIFICATION

V0.17

N

Preliminary
Dec, 1998
Information contained herein is
subject to change without notice.

AC-DC Driver / LM2453
Monolithic Triple 5.5 nS CRT Driver with Integrated Clamp and G1 Blanking

This is the Preliminary Product Requirements Specification for the ACDC driver. It is not a datasheet: the parameters defined in this document specify the design target value for critical performance attributes of the device, and the range of acceptable deviation from this target that will not affect the Product Business Case. Any parameter falling outside of the range specified should be reviewed against the targeted application and market, in order to ensure that the business case is still valid.

DO NOT COPY

FEATURES:

5.5ns low power driver (similar to Lm2415)

Integrated active clamp circuit

Integrated Vertical blank G1 drive circuit

Video-plex ™ interface to LM1253 OSD Pre-amp for low complexity / high integration applications

Single HV supply (80v) – self generating 120v boost supply

External System voltage reference

1.0 General Description

The ACDC driver is an integrated high voltage triple CRT driver circuit designed for use in color monitor applications. The IC contains three high gain, differential input, high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to -60 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

Integrated with the driver is triple clamp circuit for DC recovery of each of the AC coupled outputs. The DC clamp circuit amplifies the clamp signal that is multiplexed on the video signal input. The DC clamp amplifiers are high gain, differential input, high input impedance amplifiers, setting a low impedance DC level at the clamp output which can be used to restore the DC level of the cathode drive. Each channel has a gain that is internally set to +72.

Also integrated within the package is a 45vp-p vertical blanking driver that is designed to drive the vertical retrace blanking signal to the G1. This is a current limited, low impedance output capable of driving normal G1 decoupling capacitances via an external resistor.

The output of the G1 driver can also be used to drive a voltage boost capacitor (10uF). When connected between the G1 drive output and the 120v supply input pin, a 120v boost supply is achieved which can be used to drive the internal DC clamp circuit, thereby eliminating the requirement for a 120V clamp supply. When the first vertical blanking pulse is received, the G1 drive output enters a current limited latched state until the 120v boost capacitor is fully charged. Thereafter, the G1 output pulses in response to the vertical blanking pulse received on the multiplexed Vref signal line.

The IC is packaged in an industry standard 15 lead TO-220 molded plastic power package.

The input signal interface to the IC is a multiplexed signal containing both clamp and video signal information, relative to an external 1.8v DC reference.

2.0 Intended Applications

The ACDC driver has a nominal tr/tf of 5.5ns. With normal amounts of external inductive peaking, this device is targeted for use in applications with pixel clocks up to around 110MHz. This makes the device ideally suited for 1280x1024 at 75Hz. (140MHz pixel clock). Some customers may be able to obtain useful performance up to 160MHz pixel clock, or 1280x1024 at 85Hz., depending upon the individual customers criteria for how much bandwidth is required for a given application.

Target applications running at these speeds are mid range 15" and 17" monitors.

3.0 Basic Application Schematic and Connection Diagrams

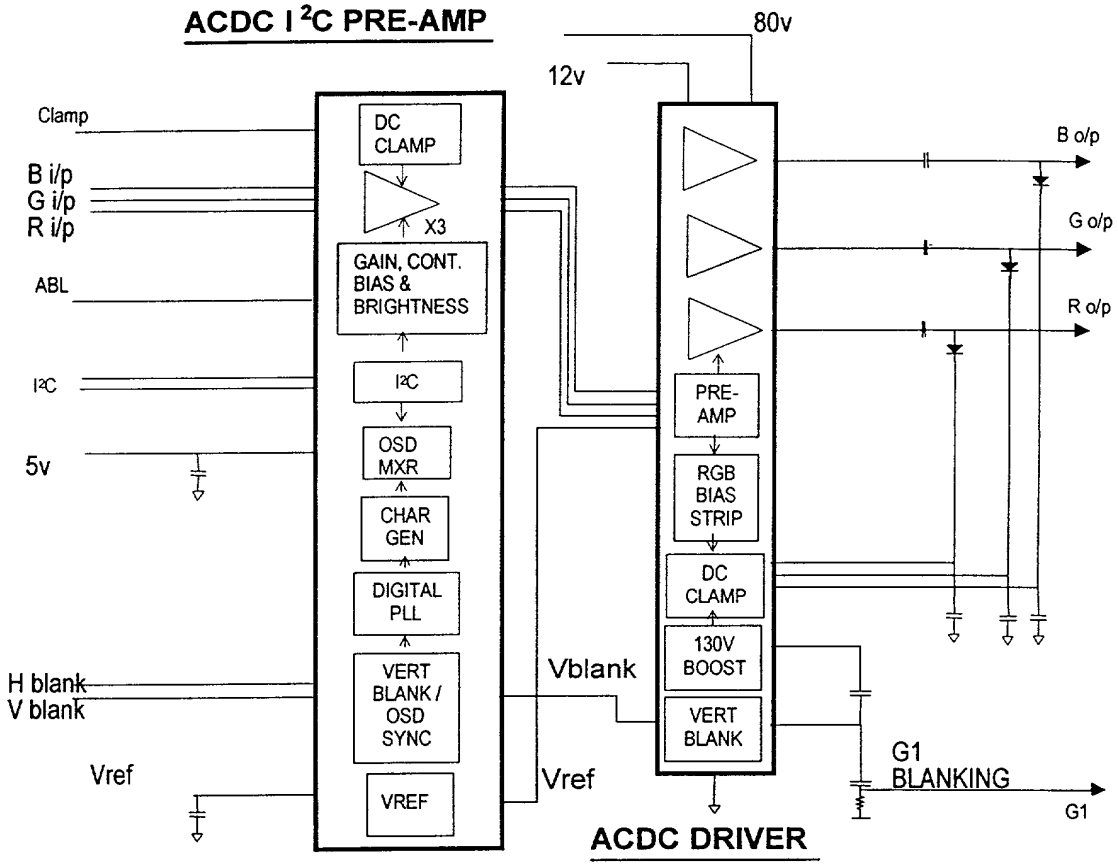
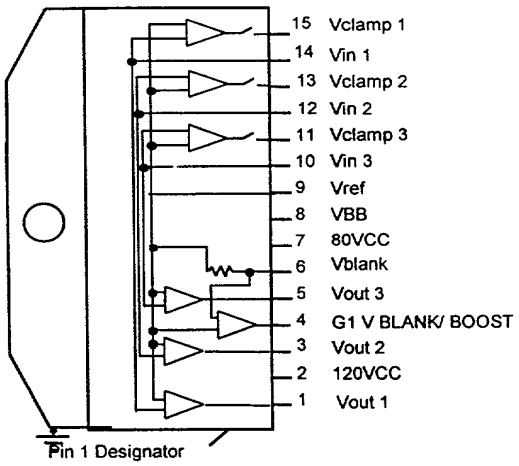


Figure 1. Simplified Schematic Diagram



Note1: Tab is GND

Note 2: PIN OUT SUBJECT TO CHANGE

Figure 2. Top View

4.0 Special Features

The ACDC system using the National Video-plex™ multiplexed video signal to send the video signal and DC clamp level from preamplifier to driver. The basic signal scheme is shown in figure 3.

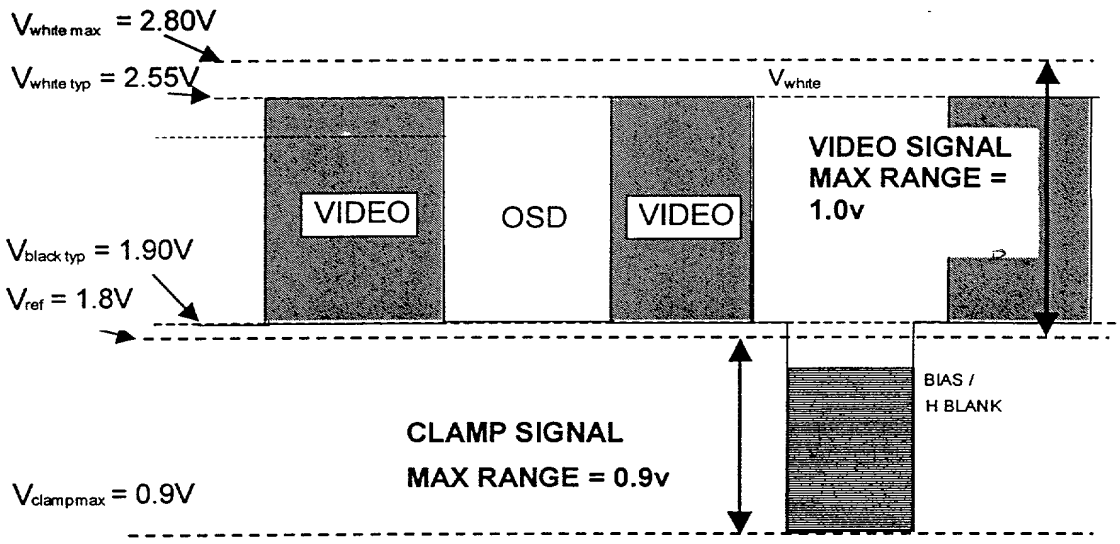


Figure 3. ACDC SYSTEM TYPICAL VIDEO SIGNAL

The response to the video and clamp amplifiers to the video-plex$_t^m$ signal is shown in figure 4.

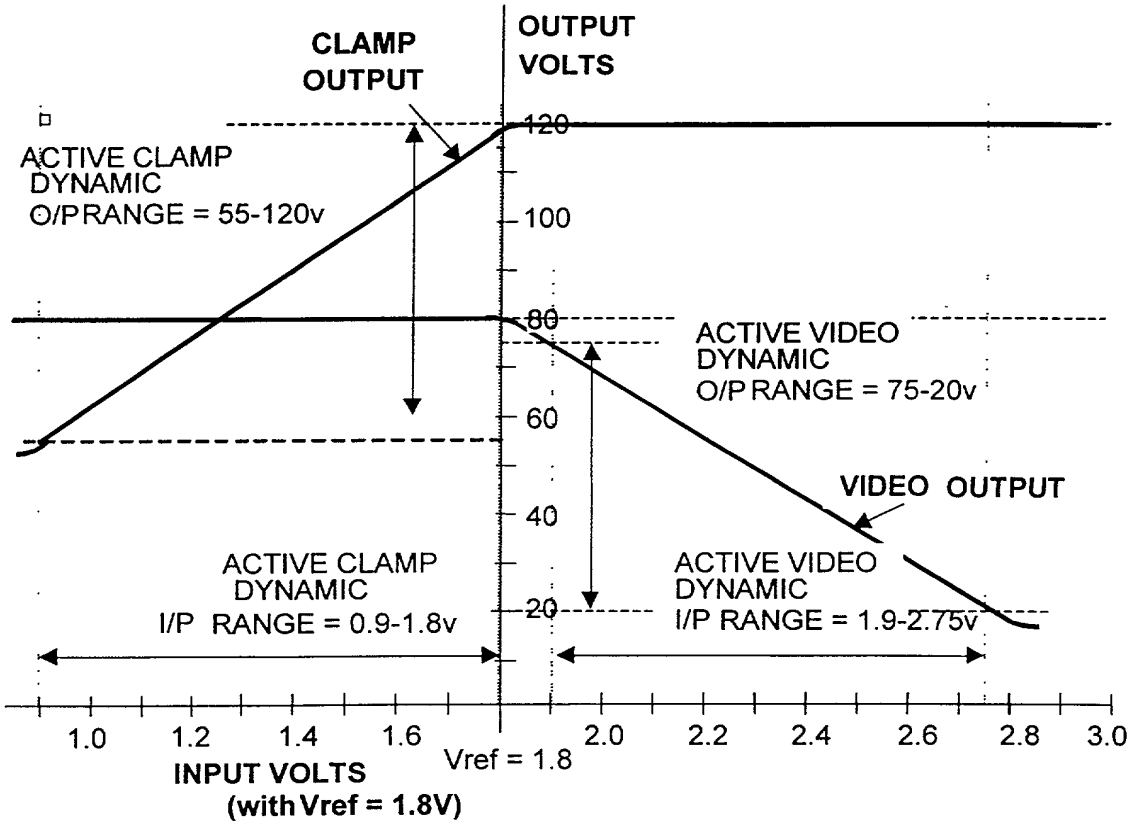


Figure 4: DC I/O Transfer Characteristic for Driver and Clamp Amplifiers
(Test Conditions: Vref = 1.8v, Vcc1 = 80v, Vcc2 = 120v, Vbb = 12v)

Figure 5 shows the operation of the G1 blanking output in combination with the 120V boost operation during start up.

DO 4207 " 65/85/50

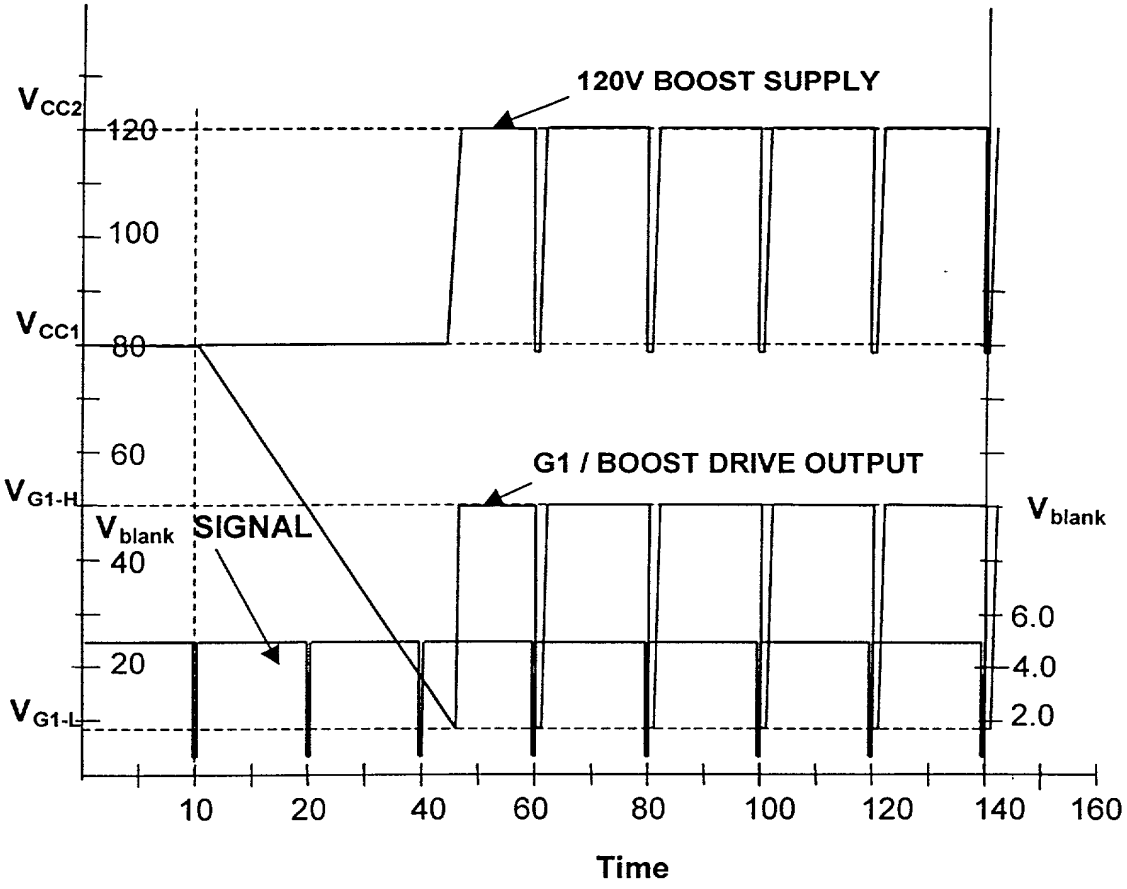


Figure 5: 120v BOOST SUPPLY / G1 BLANKING PULSE OUTPUT AT START UP, SHOWING INITIAL CURRENT LIMITED CHARGE UP

DO/ZOT 'SE/S8S/SSO

Limits of Absolute Maximum Ratings (Notes 1 & 3)

The following parameters will be specified in the data sheet; the specification limits of the device should be within the range specified below:

80v Voltage, V_{CC1}	Equal to or better than +90 V
120v Supply $V_{CC\ 2}$	Equal to or better than +130 V
Bias Voltage, V_{BB}	Equal to or better than +16 V
Input Voltage, V_{IN}	Equal to or better than 0 V to 6 V
Input Reference Voltage, V_{REF}	Equal to or better than 0 V to 6 V
VBLANK Input Voltage, V_{BLANK}	Equal to or better than 0 V to V_{BB} V
Storage Temperature Range, T_{STG}	Equal to or better than -65 °C to +150 °C
Lead Temperature (Soldering, <10 sec.)	Equal to or better than 300 °C
ESD Tolerance, Human Body Model	Equal to or better than 2kV min
ESD Tolerance, Machine Model	Equal to or better than 200V min

Note: the product will be stress tested during manufacturing to 96v at the 80v V_{cc1} supply input. This will stress the V_{cc2} input to 136v

Limits of Operating Ranges (Note 2)

V_{CC1}	Equal to or better than +60 V to + 85V
V_{CC2}	Equal to or better than V_{cc1} to + 125V
V_{BB}	Equal to or better than +8 V to +15 V
V_{IN}	Equal to or better than +1 V to +3 V
V_{REF}	Equal to or better than +1 V to +3 V
VBLANK Input Voltage, V_{BLANK}	Equal to or better than 0 V to 5.5 V
V_{out}	Equal to or better than +15 to +75 V
V_{clamp}	Equal to or better than +50 to +120 V
Tjmax	Equal to or better than +150C

DESIGN FOR ROBUSTNESS:

The ACDC driver shall be internally laid out to enable the use of series peaking capacitors, and all outputs will use the same size ESD diodes as the 2405C. Any unused devices will be connected with metal in such a manner as to prevent parasitic SCR effects.

DS012700-95

AC DRIVER Electrical Characteristic Targets and Limits (See Figure 6 for Test Circuit)

Unless otherwise noted: V_{CC} = +80 V, V_{BB} = +12 V, V_{IN} = 2.3VDC, C_L = 8 pF, Output = 40 V_{PP} at 1 MHz, T_C = 50 °C. Vref =1.80v SW1 open

HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable
0 is a target value means that the ideal value is as low as possible.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
I_{CC1MAX}	Maximum Supply Current	All 3 Channels, No Output Load	NA	45		mA
I_{BBMAX}	Maximum Bias Current	All three channels	NA	0	60	mA
V_{OUTTYP}	Typical DC Output Voltage	No AC Input Signal	48	50	52	V_{DC}
ΔV_{OUTTYP}	Variation in DC Output Voltage about typical	No AC Input Signal	NA	0	+/-3v	V_{DC}
A_{vtyp}	Typical DC Voltage Gain	No AC Input Signal	-62	-65	-68	
ΔA_{vtyp}	Variation of DC Voltage Gain about typical	No AC Input Signal	NA	0	+/-5	
ΔA_{vgmtyp}	Typical Gain Matching between channels	Note 4, No AC Input Signal	NA	0	1.0	dB
LE_{typ}	Typical Linearity Error	Notes 4, 5, No AC Input Signal	NA	0	8	%
t_{rtyp}	Typical Rise Time	10% to 90%	5.2	5.5	5.7	nS
Δt_r	Variation in rise time about typical		NA	0	+/-25	%
Δt_{rch-ch}	Channel to Channel rise time matching	Note 7	NA	0	+/-15	%
t_{ftyp}	Typical Fall Time	90% to 10%	5.2	5.5	5.7	nS
Δt_f	Variation in fall time about typical		NA	0	+/-25	%
Δt_{fch-ch}	Channel to Channel fall time matching	Note 8	NA	0	+/-15	%
OS	Typical Overshoot	Rising Edge Falling Edge	NA	0 0	8 2	%
OS_{max}	Maximum Overshoot	Rising Edge Falling Edge	NA	-0 0	10 6	%
dt/dT	Variation in response time with temperature	Note 9	NA	0	+/-0.14	%/C

dt/dC_l	Variation in response time with load capacitance	Note 10	NA	0	+/-2	%/pf
dV_{out} / dV_{ref}	Variation in output with changes inV_{ref}	For 1.6v < Vref <2.0v	-5	0	5	V/V
dV_{out} / dV_{bb}	Variation in output with changes inV_{bb}		-0.5	0	0.5	V/V
dV_{out} / dV_{cc1}	Variation in output with changes inV_{cc1}		-1	0	1	V/V
dV_{out} / dV_{cc2}	Variation in output with changes inV_{cc2}		-1	0	1	V/V
	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/ Cathode
	Thermal Smear	Tested in Monitor with NSC Neck Board and ACDC Preamp	NA	0	None Visible	
	Overvoltage Stress	V_{CC} = 96V, V_{BB} = 16V, V_{IN} = Vref to 4V, one cycle V_{CC} = 80V, V_{BB} = 12V, V_{IN} = Vref to 4V, 1000 cycles	No damage No damage	NA	NA	
R_{dd}	Die Differentiator Resistance	Built input resistance between input and Vref	9	10	11	kohm

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Linearity Error is the variation in dc gain from Vin=2.0 volts to Vin=2.6 volts.

Note 6: Input from signal generator: t_r, t_f < 1 nS.

Note 7: $\Delta t_{rch\text{-}ch} = 200*(t_{rcha} - t_{rchb})/(t_{rcha}+t_{rchb})\%$

Where:

- channel a and channel b are <u>any</u> two channels within the same device
- t_{rcha} and t_{rchb} refers to the rise time of channel a and channel b.

Note 8: $\Delta t_{fch\text{-}ch} = 200*(t_{fcha} - t_{fchb})/(t_{fcha}+t_{fchb})\%$

Where:

- channel a and channel b are <u>any</u> two channels within the same device
- t_{fcha} and t_{fchb} refers to the fall time of channel a and channel b.

Note 9: $dt/dT = 200*(t_{100C} - t_{40C})/ ((t_{100C} + t_{40C})*60)$ %/C,

Where:

- t_{40C} is the rise or fall time at 40C
- t_{100C} is the rise or fall time at 100C case temperature.

Note 10: $dt/dC_l = 200*(t_{20pf} - t_{8pf})/ ((t_{20pf} + t_{8pf})*12)$ %/pf

Where:

- t_{20pf} is the rise or fall time with 20pf load
- t_{8pf} is the rise or fall time with 8pf load.

005720 of 005949

Note 11: Tested with appropriate external protection network that maintains product performance, as defined in the datasheet.

OTHER PRODUCT REQUIREMENTS

Crossover Distortion:

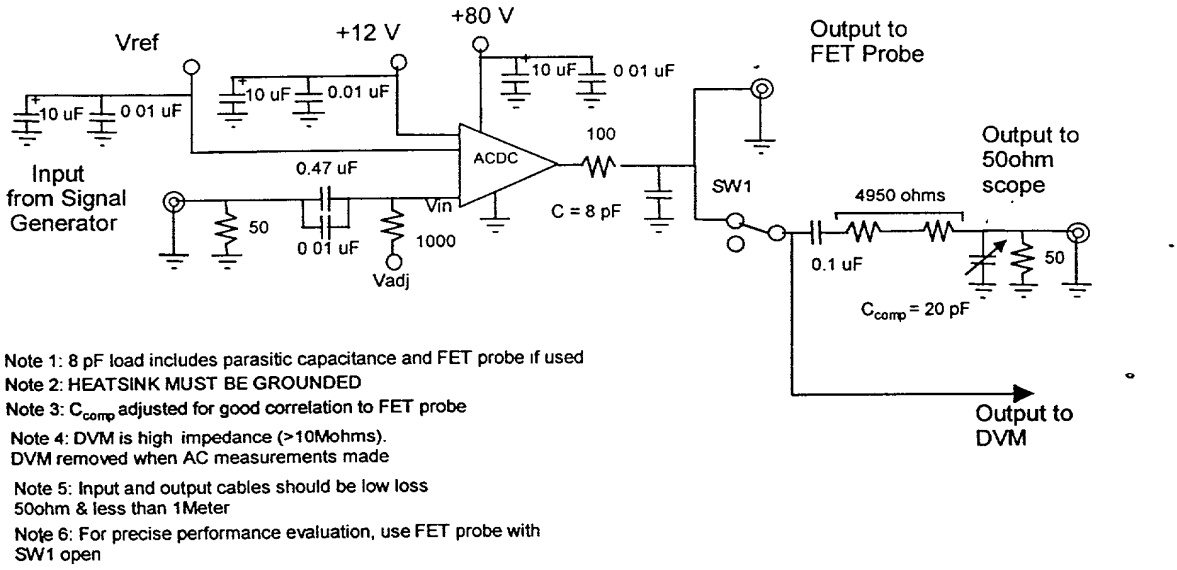
The device should have a class AB output stage, and should exhibit no small signal cross-over distortion without the need for any external resistive load. The small signal rise and fall times at 1vp-p should be within +/- 20% of the large signal values.

Gain Compression

Any change in bandwidth with output signal magnitude should be smooth and continuous, with no rapid changes in gain.

- The gain should not vary by more than +/-2dB over an output range of 1-40V at any given frequency for all frequencies below the 40v -3dB bandwidth.

DRIVER Test Circuit



Note 1: 8 pF load includes parasitic capacitance and FET probe if used
Note 2: HEATSINK MUST BE GROUNDED
Note 3: C_{comp} adjusted for good correlation to FET probe
Note 4: DVM is high impedance (>10Mohms). DVM removed when AC measurements made
Note 5: Input and output cables should be low loss 50ohm & less than 1Meter
Note 6: For precise performance evaluation, use FET probe with SW1 open

FIGURE 6. Test Circuit (One Channel)

Figure 6 shows a typical test circuit for evaluation of the ACDC DRIVER. For precise evaluation, a calibrated FET probe should be used. This circuit is also allows testing of the ACDC DRIVER in a 50 ohm environment without the use of an expensive FET probe. The 4950 ohm resistor at the output forms a 200:1 voltage divider when connected to a 50 ohm load. Ccomp must be adjusted for equivalent performance to the FET probe, though performance may be affected by the effect of the load of the 5k.

DC CLAMP Electrical Characteristic Targets and Limits (See Figure 7 for Test Circuit)
Unless otherwise noted: V_{CC1} = +80 V, V_{CC2} = +120 V, V_{BB} = +12 V, V_{IN} = 1.8VDC, T_C = 50 °C, Vref =1.80v, SW1 open.

HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.
Note: NA means not applicable
0 is a target value means that the ideal value is as low as possible.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
I_{CC2MIN}	Maximum DC Supply Current at Voutmin	Per Channel, No AC input signal, Vin=1.25v	NA	0	1.2	mA
I_{CC2MAX}	Maximum DC Supply Current at Voutmax	Per Channel, No AC input signal, Vin=1.75v	NA	0	0.1	mA
V_{OUTTYP}	Typical DC Output Voltage	No AC Input Signal, Vin=1.5V	88	90	92	V_{DC}
ΔV_{OUTTYP}	Variation in DC Output Voltage about typical	No AC Input Signal, Vin=1.5v	NA	0	+/-3v	V_{DC}
A_{vtyp}	Typical DC Voltage Gain	No AC Input Signal	72	75	78	
ΔA_{vtyp}	Variation of DC Voltage Gain about typical	No AC Input Signal	NA	0	+/-4	
ΔA_{vgmtyp}	Typical Gain Matching between channels	No AC Input Signal	NA	0	1.0	dB
LE_{typ}	Typical Linearity Error	No AC Input Signal, See Note 4	NA	0	8	%
t_{ftyp}	Typical Fall Time	90% to 10%	0	0	500	nS
OS_{max}	Maximum Overshoot	Falling Edge	0	0	None	%
Rout	Typical output resistance	Vin = 1.5v, Clamp active See Note 5 and test circuit	0	0	200	ohms
dV_{ou} / dV_{bb}	Variation in output with changes inV_{bb}		-0.5	0	0.5	V/V
dV_{out} / dV_{ref}	Variation in output with changes inV_{ref}	For 1.6v < Vref <2.0v	-5	0	5	V/V
dV_{out} / dV_{cc}	Variation in output with changes inV_{cc}		-1	0	1	V/V
dV_{ou} / dV_{cc2}	Variation in output with changes inV_{cc2}		-1	0	1	V/V
dV_{out}/dT	Variation in output with temperature	At any output voltage setting, compared to Vin=1.5v at 25C Tcase =15C-100C	0	0	+/-0.25	V

	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/ Cathode

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.
Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.
Note 3: All voltages are measured with respect to GND, unless otherwise specified.
Note 4: Linearity Error is the variation in dc gain from Vin=1.3 volts to Vin=1.7 volts.
Note 5: Calculated value when SW1 is closed:

$$Rout = \frac{(V_{open} - V_{closed}) * 10Kohm}{V_{closed}}$$

Where:

- V_{open} is the output voltage when SW1 is open
- V_{closed} is the output voltage when SW1 is closed

Clamp AmplifierTest Circuit

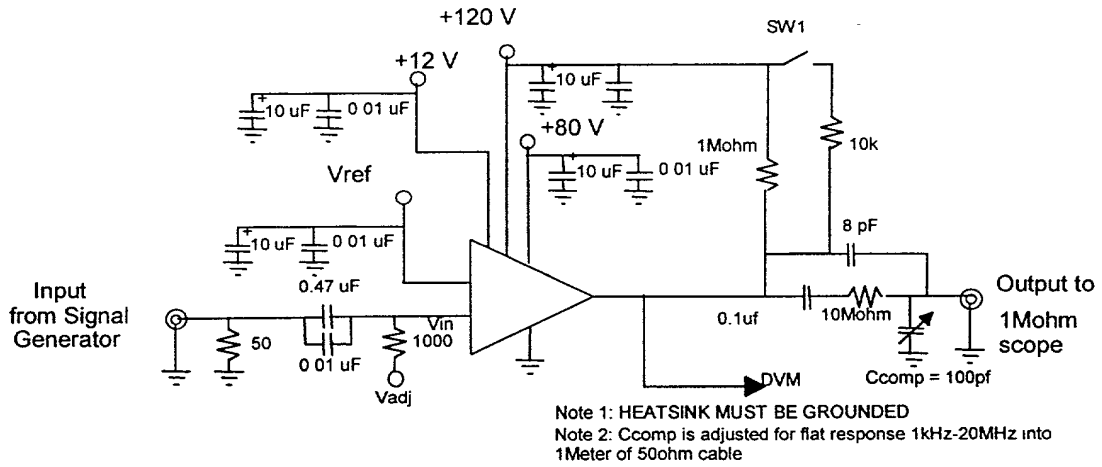


FIGURE 7. Test Circuit (One Channel)

Figure 7 shows a typical test circuit for evaluation of the ACDC clamp amplifier. A high impedance DVM (>10Mohm) should be used for DC measurements at the outputs. Vadj is adjusted to the value Vin as specified in the specification table.

G1 DRIVER/BOOST Electrical Characteristic Targets and Limits (See Figure 8 for Test Circuit)

Unless otherwise noted: V_{CC} = +80 V, V_{BB} = +12 V, V_{IN} = 2.3VDC, C_L = 8 pF, Output = 40 V_{PP} at 1 MHz, T_C = 50 °C. Vref =1.80v , SW1,SW2 open

HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable
0 is a target value means that the ideal value is as low as possible.
Spread means variation of parameter in production with tolerance

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
V_{G1-H}	Typical G1 High output voltage	V_{blank} input low, see Note 8. See figure 5	48	50	52	V_{DC}
V_{G1-L}	Typical G1 Low output voltage	V_{blank} input high, see Note 8. See figure 5	7	9	11	V_{DC}
V_{G1pp}	Typical G1 output p-p		39	41	43	
ΔV_{G1pp}	Spread of G1 output p-p about typical		0	0	+/-3	V
ΔV_{G1pp} /dT	Variation in G1 output with temperature	At any output voltage setting, compared to 25C Tcase =15C-100C	0	0	+/-0.25	V
I_{G1max}	Typical short term maximum current sink at G1 output	First blanking pulse during start up. See figure 5	20	25	35	mA
ΔI_{G1max}	Spread in maximum current sink at G1 output		0	0	5	mA
V_{ref} I_{max}	Maximum operational input current of V_{ref}		300	NA	NA	uA
$dV_{r,g,bout}$/ dI_{ref}	Variation in video output voltage with variation in V_{ref} load	See note 6	0	0	250	mV/mA
V_{G1th}	G1 blanking input threshold	See note 7	Vref – 0.25	Vref	Vref +0.25	V
ΔV_{G1th}	Spread in G1 blanking input threshold	Over production spread	0	0	+/-0.25	V
V_{ref} R_{in}	Typical input resistance of V_{ref}	V_{ref} < 1.8v	10	NA	NA	kohms
$V_{120BOOST}$	Typical 120V boost supply	SW1 open	118	120	125	V
$\Delta V_{120BOOST}$	Spread in 120V boost supply	SW1 open	0	0	+/-5	V

DO NOT SCALE DRAWING

ΔV_{G1pp} /dT	Variation in 120V boost supply with temperature	At any output voltage setting, compared to 25C Tcase =15C-100C	0	0	+/-0.5	V
T_{G1rtyp}	Typical Rise Time	10% to 90%, see Note 8	0	0	20	uS
T_{G1ftyp}	Typical Fall Time	10% to 90%, see Note 8	0	0	5	uS
$d V_{120BOOST} / dV_{bb}$	Variation in 120v boost supply with changes inV_{bb}		0	0	+/-1	V/V
$d V_{120BOOST} / dV_{cc}$	Variation in 120v boost supply with changes inV_{cc}		0	0	+/-1	V/V
	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/ Cathode

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Calculated value of Vref output resistance when SW2 is closed:

$$Rout = \frac{(V_{closed} - V_{open}) * 10kohm}{\{2.8 + V_{open} - (2 * V_{closed})\}}$$

Where:

- V_{open} is the Vref output voltage when SW2 is open
- V_{closed} is the Vref output voltage when SW2 is closed

Note 6: Calculated variation in video output voltage when SW2 is closed:

$$dV_{r,g,bout} / dI_{ref} = \frac{(V_{r,g,b\ open} - V_{r,g,b\ closed}) * 10kohm}{2.8 - V_{ref}}$$

Where:

- $V_{r,g,b\ open}$ is any video output voltage when SW2 is open
- $V_{r,g,b\ closed}$ is any video output voltage when SW2 is closed

Note 7: Calculated value of 120V boost output resistance when SW1 is closed:

$$Rout = \frac{(V_{open} - V_{closed}) * 390kohm}{V_{closed}}$$

Where:

- V_{open} is the 120v boost output voltage when SW1 is open
- V_{closed} is the 120v boost output voltage when SW1 is closed

Note 8: Input from signal generator: 2vp-p pulse: t_{high} = 300us, t_{low} =10ms, 2v p-p. rise/fall time <0.1us

00720114 6E/8E/9E/AE/BE/CE/DE

120V Boost / G1 Drive /V_{ref} Test Circuit

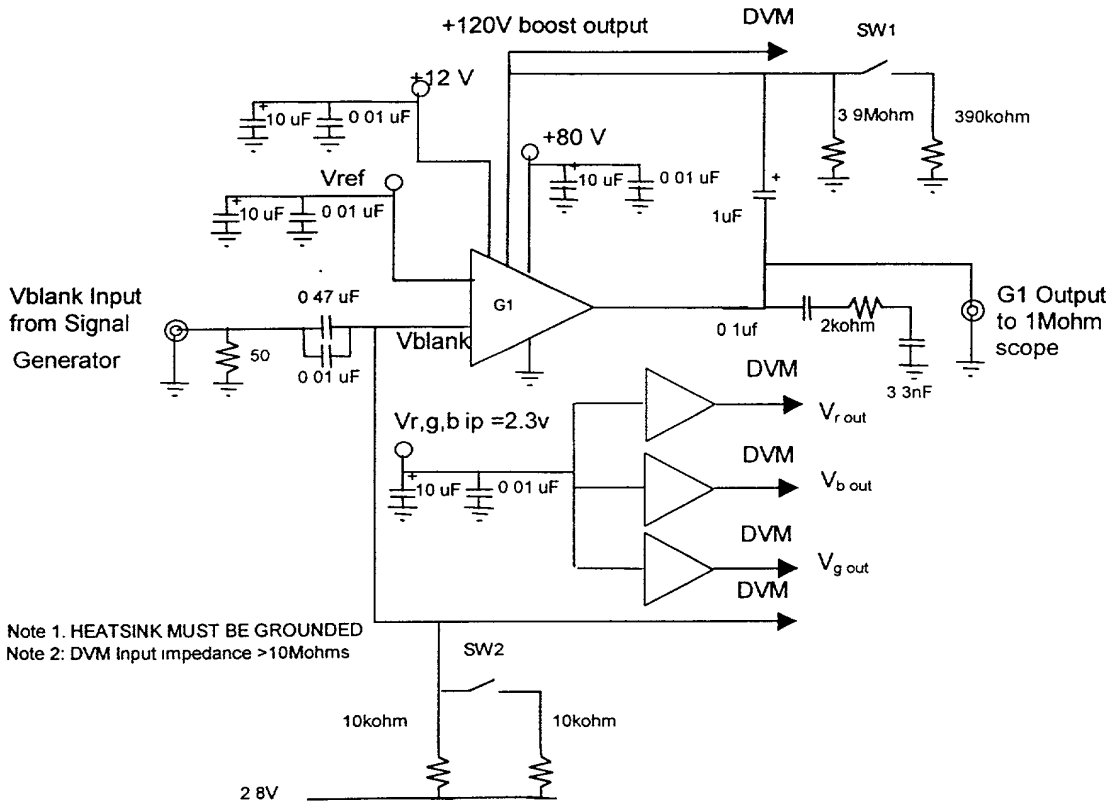


FIGURE 8. 120V Boost /G1 / V_{ref} Drive Test Circuit

REVISION HISTORY:

V0.14 Sept 98:
Figure 6 changed to show FET probe as preferred AC measurement method
Polarity of Vblank pulse changed to negative going. Table and Figures 5 & 8 changed to reflect these changes.
V0.15 10/13/98: Figure 2 changed to include pin out of device. Added feature list on page 2.
V0.17 12/24/98: Spec changed to reflect removing Vref. Gain of clamp circuit reduced to 72.

EXPRESS MAIL NO.: EL563098702US

APPENDIX B

09/07/00 - 09/08/00

00201 "6E286960

National Semiconductor

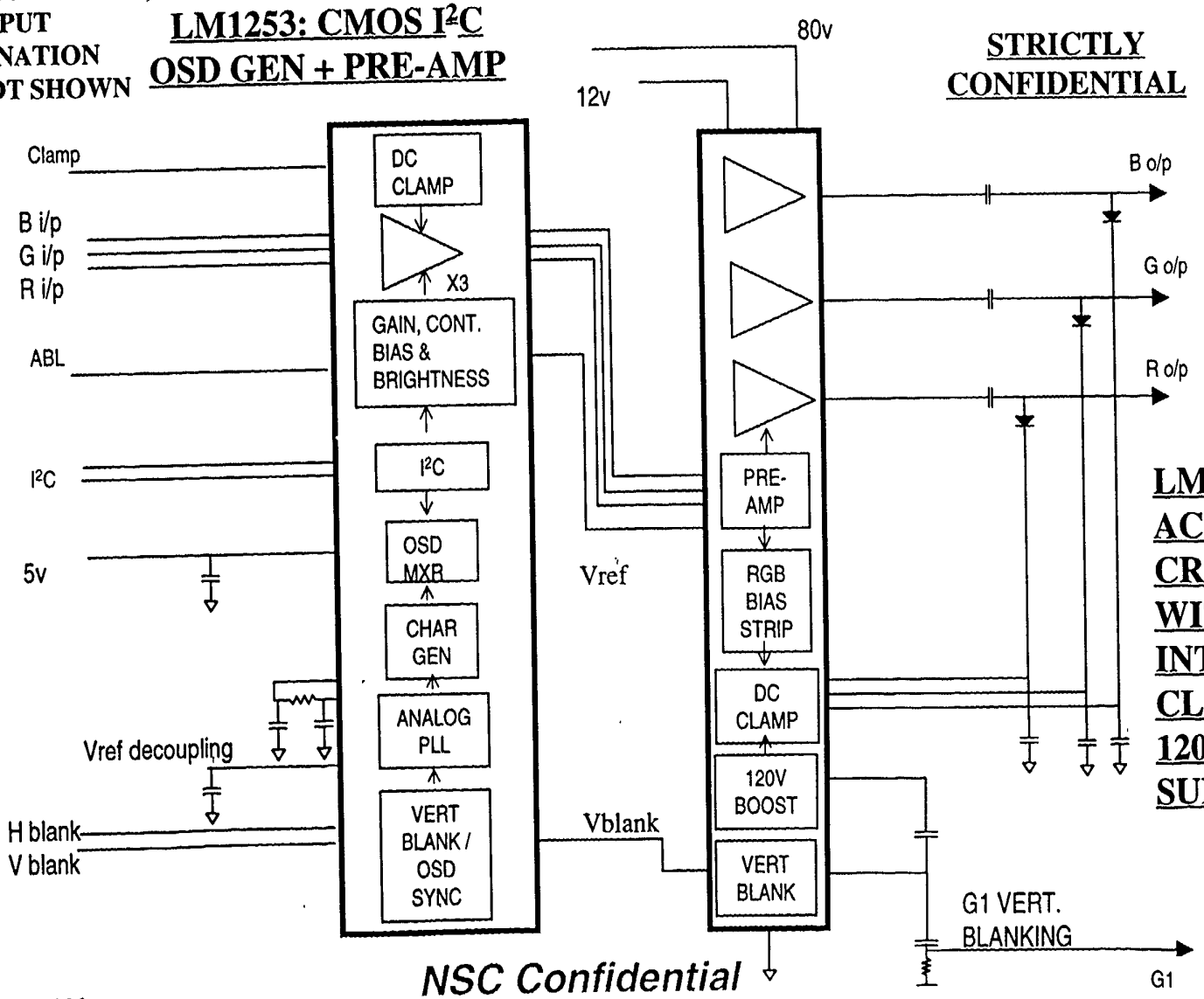
AC2DC

NEW AC2DC SYSTEM

ARC PROTECTION, ESD, INPUT TERMINATION ETC NOT SHOWN

LM1253: CMOS I²C OSD GEN + PRE-AMP

STRICTLY CONFIDENTIAL



LM2453: AC COUPLED CRT DRIVER WITH INTEGRATED CLAMP AND 120V BOOST SUPPLY

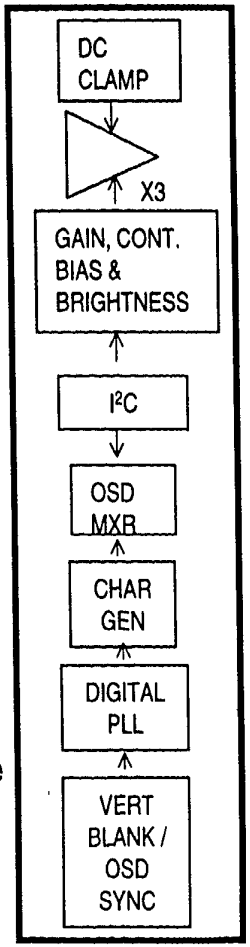
NSC Confidential

6/25/99 AJM

00720T"6E786960

LM1253: I²C OSD GENERATOR + PRE-AMP

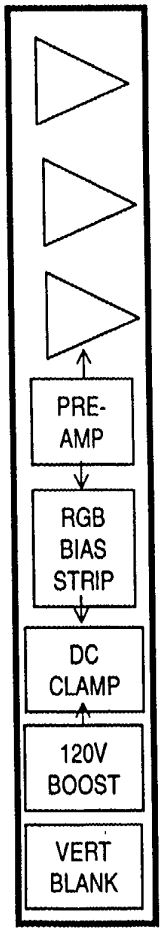
- 0.35u 5v CMOS OSD/PRE-AMP - LM1253
  - state of the art process
  - many future integration possibilities (eg uC, USB, DDC etc)
  - first device in new family of OSD-Preamps
- Single low cost package (28pin DIL)
- I²C controlled OSD and all pre-amp functions
- *Videoplex* driver interface video signal
  - OSD
  - DC bias and brightness
  - H blank
  - Video signal
- Single 5v, 0.25mA supply
  - low power standby mode
- Easy interface to Hflyback, Vflyback, ABL
  - internal clamping - only one external resistor for flyback interface
  - vertical blanking duration controlled by digital counter
- High input impedance - low smear
- Bi-directional output drive - good symmetry



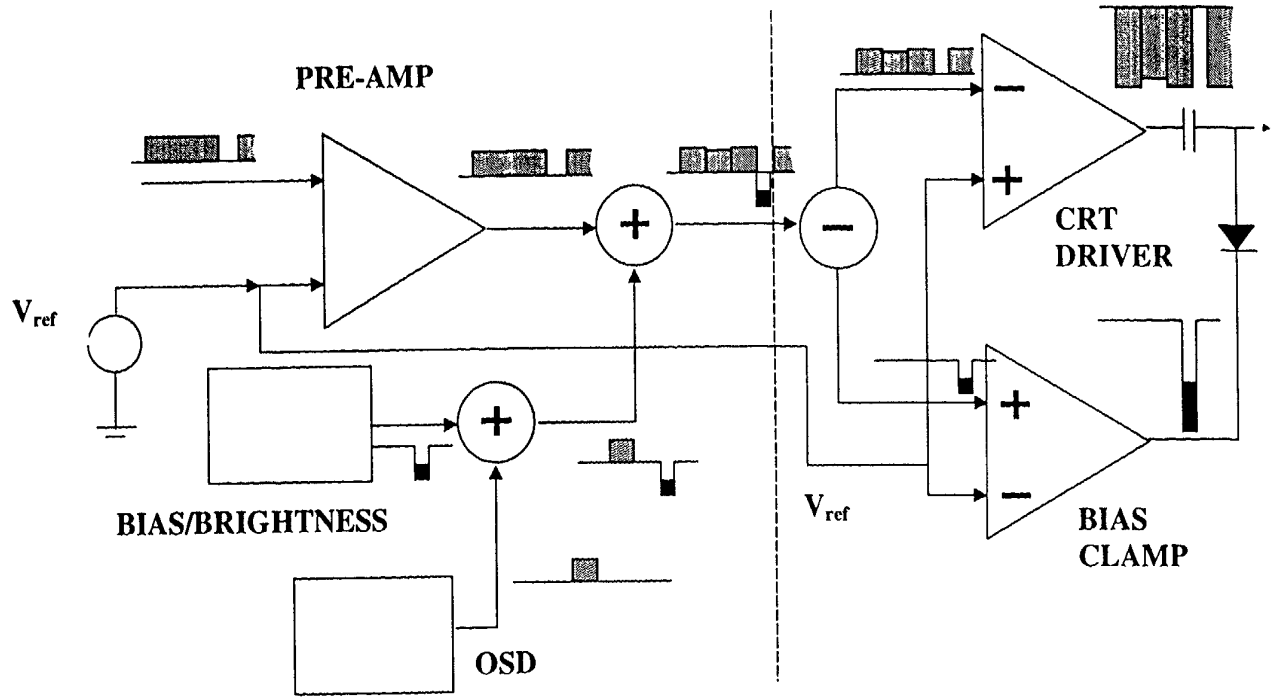
00720T"6Z786960

INTEGRATED AC DRIVER/CLAMP

- Similar to today's open loop AC driver designs
  - uses existing NSC low power technology (eg LM2415 etc)
  - 75-85v Vcc for lowest AC power
  - higher gain (50X)
  - differential input to give good DC stability at higher gain
- DC bias clamp function
  - ultra low power operation
  - >60V DC adjustment range
  - allows brightness and bias functions
- G1 vertical blank generator / 120v capacitor boost circuit
  - 40v p-p vertical blanking pulse
  - boost circuit for bias clamp circuit



AC$_2$DC SYSTEM BLOCK DIAGRAM



PRE-AMP

DRIVER/CLAMP

00/201"6E/86960

National Semiconductor

AC2DC

ACDC VALUE PROPOSITION v LM1279

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						$1.20	$1.35	$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			$0.20	$0.35	$0.50
PWM FILTERS			8	8			$0.04	$0.08	$0.10
PREAMP	LM1279						$0.45	$0.55	$0.65
256char PWM OSD GEN	MYSON / MOTO						$0.85	$1.10	$1.45
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	$0.10	$0.12	$0.15
PCB MATERIAL SAVINGS						20-30%	$0.02	$0.08	$0.15
SMALLER EMI SHIELD						20-30%	$0.02	$0.08	$0.15
G1 VERT BLANKING		1	4	1			$0.03	$0.05	$0.07
G1 BRIGHTNESS CONTROL		1	4	1			$0.03	$0.05	$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		$0.03	$0.06	$0.08
H FLYBACK LEVEL CLAMPS				1	2		$0.01	$0.02	$0.03
PRE-AMP DC DECOUPLING CAPS				6			$0.04	$0.06	$0.08
TOTAL SYSTEM VALUE							**$3.02**	**$3.95**	**$4.98**

NSC Confidential

6/25/99 AJM

00720T"6E786960

National Semiconductor

AC2DC

ACDC VALUE PROPOSITION v TDA4886

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						$1.20	$1.35	$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			$0.20	$0.35	$0.50
PWM FILTERS			4	4			$0.02	$0.04	$0.05
I2C PREAMP	TDA4886						$0.70	$0.80	$0.90
256char OSD GEN	MYSON / MOTO						$0.70	$0.80	$1.00
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	$0.10	$0.12	$0.15
PCB MATERIAL SAVINGS						20-30%	$0.02	$0.08	$0.15
SMALLER EMI SHIELD						20-30%	$0.02	$0.08	$0.15
G1 VERT BLANKING		1	4	1			$0.03	$0.05	$0.07
G1 BRIGHTNESS CONTROL		1	4	1			$0.03	$0.05	$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		$0.03	$0.06	$0.08
H FLYBACK LEVEL CLAMPS				1	2		$0.01	$0.02	$0.03
PRE-AMP DC DECOUPLING CAPS				6			$0.04	$0.06	$0.08
TOTAL SYSTEM VALUE							**$3.10**	**$3.86**	**$4.73**

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AC2DC

ACDC VALUE PROPOSITION v LM1279

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						$1.20	$1.35	$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			$0.20	$0.35	$0.50
PWM FILTERS			8	8			$0.04	$0.08	$0.10
PREAMP	LM1279						$0.45	$0.55	$0.65
256char PWM OSD GEN	MYSON / MOTO						$0.85	$1.10	$1.45
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	$0.10	$0.12	$0.15
PCB MATERIAL SAVINGS						20-30%	$0.02	$0.08	$0.15
SMALLER EMI SHIELD						20-30%	$0.02	$0.08	$0.15
G1 VERT BLANKING		1	4	1			$0.03	$0.05	$0.07
G1 BRIGHTNESS CONTROL		1	4	1			$0.03	$0.05	$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		$0.03	$0.06	$0.08
H FLYBACK LEVEL CLAMPS				1	2		$0.01	$0.02	$0.03
PRE-AMP DC DECOUPLING CAPS				6			$0.04	$0.06	$0.08
TOTAL SYSTEM VALUE							**$3.02**	**$3.95**	**$4.98**

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National Semiconductor

AC2DC

ACDC VALUE PROPOSITION v TDA4886

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						$1.20	$1.35	$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			$0.20	$0.35	$0.50
PWM FILTERS			4	4			$0.02	$0.04	$0.05
I2C PREAMP	TDA4886						$0.70	$0.80	$0.90
256char OSD GEN	MYSON / MOTO						$0.70	$0.80	$1.00
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	$0.10	$0.12	$0.15
PCB MATERIAL SAVINGS						20-30%	$0.02	$0.08	$0.15
SMALLER EMI SHIELD						20-30%	$0.02	$0.08	$0.15
G1 VERT BLANKING		1	4	1			$0.03	$0.05	$0.07
G1 BRIGHTNESS CONTROL		1	4	1			$0.03	$0.05	$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		$0.03	$0.06	$0.08
H FLYBACK LEVEL CLAMPS				1	2		$0.01	$0.02	$0.03
PRE-AMP DC DECOUPLING CAPS				6			$0.04	$0.06	$0.08
TOTAL SYSTEM VALUE							**$3.10**	**$3.86**	**$4.73**

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AC2DC

LM1253

OSD GENERATOR AND PRE-AMP

FAE TRAINING SPECIFICATION

THIS DOCUMENT IS A PRELIMINARY SPECIFICATION FOR THE LM1253 FOR THE PURPOSE OF FAE TRAINING. ALL INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE. THE PIN-OUT FOR THE DEVICE IS NOT FINALIZED.

THIS DOCUMENT IS CONFIDENTIAL AND THE INFORMATION CONTAINED WITHIN SHOULD NOT BE DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR AGREEMENT.

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7/2/99

V0.1

AUTHOR: Andy Morrish

National Semiconductor

AC2DC

Preliminary

Mar, 1999

Information contained herein is subject to change without notice.

AC-DC OSD GENERATOR AND PRE-AMP OVERVIEW

MONOLITHIC TRIPLE 150MHZ I^2C CRT PREAMP WITH INTEGRATED OSD

This is a preliminary product specification for the LM1253 pre-amp and OSD generator to be used in the AC_2DC^{TM} system. The parameters defined in this document specify the design target value for critical performance attributes of the device.

FEATURES:

150MHz preamplifier with full video signal parametric control

Channel Gain corrected Brightness and OSD control

Videoplex™ interface to AC_2DC^{TM} driver

OSD mixing with 64 out of 512 color mask programmable selection

190 two-color ROM based Character Fonts with individual character attribute

64 four-color ROM based Character Fonts with individual character attribute

Programmable window size with up to 512 character and line definition codes

Support for 2 independent Display Windows (size of each window is configurable)

Programmable start position for each Display Window

Programmable Resolutions: from 512 to 960 pixels per line in 64 pixel increments

Programmable Character Height, with automatic height control with mode change

Programmable blank line spacing between each display character row

Maximum Pixel clock of 92.2 MHz, maximum line rate 125kHz

I^2C compatible interface to system micro-controller

Programmable color Windows95™ style 'button boxes', shadows, borders

Programmable period vertical blanking pulse

Easy interface to H and V flyback pulses for video blanking

00/20/1 "e3/66/60

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1 PREAMPLIFIER

1.1 PRE-AMP GENERAL DESCRIPTION

The LM1253 pre-amp is an integrated high voltage triple CRT pre-amp and On Screen Display (OSD) generator. The IC is I^2C controlled, and allows control of all the parameters necessary to setup and adjust the brightness and contrast in the CRT display. In addition, it provides a programmable period vertical blanking pulse which is used to blank the G1.

The LM1253 pre-amp is designed to work in cooperation with AC_2DC™ drivers, such as the LM2453, and provides a multiplexed video signal (Videoplex™) interface to enable the DC clamp levels of AC coupled signals at the cathode to be varied in order to set up the CRT bias and to allow individual adjustment for brightness.

The OSD has a selectable palette allowing a wide selection of colors. The preset contrast level of the OSD can be controlled by I^2C to suit different CRT displays. The OSD signal is internally mixed with the video signal, before the gain section, and thus gives excellent white tracking of the OSD with the white color point setting of the video.

The Brightness settings are also mixed into the video signal before the gain matching controls and consequently give excellent white color point tracking with variations in the Brightness control.

An active horizontal blanking signal is added to the video at the output, giving excellent smear performance, and preventing video content dependant DC bias offsets as a result of high frequency over shoot.

The OSD horizontal sync and blanking signal is derived from a positive going flyback pulse. The digital section provides easy interfacing of this signal with the deflection circuits.

The vertical blanking signal is taken from the vertical sync signal, and the blanking duration is programmable. The AC_2DC ™ system is highly integrated and requires a minimal number of external components.

Black level clamping of the signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional black level clamp capacitors.

The outputs are referenced to a DC level produced by the AC_2DC ™ pre-amp, and so provide stable DC operating levels within the system without the need for additional external feedback components.

The IC is packaged in an industry standard wide body 28 lead DIL molded plastic package.

1.2 INTENDED APPLICATIONS

This device is intended for use in applications with the LM2453 AC_2DC ™ driver. This makes the device ideally suited for 1280x1024 at 75Hz. Some customers may be able to obtain useful performance up to 1280x1024 at 85Hz., depending upon the individual customers criteria for how much bandwidth is required for a given application. Target

applications running at these speeds are mid range 15" and 17" monitors.

1.3 BASIC APPLICATION SCHEMATIC AND CONNECTION DIAGRAMS

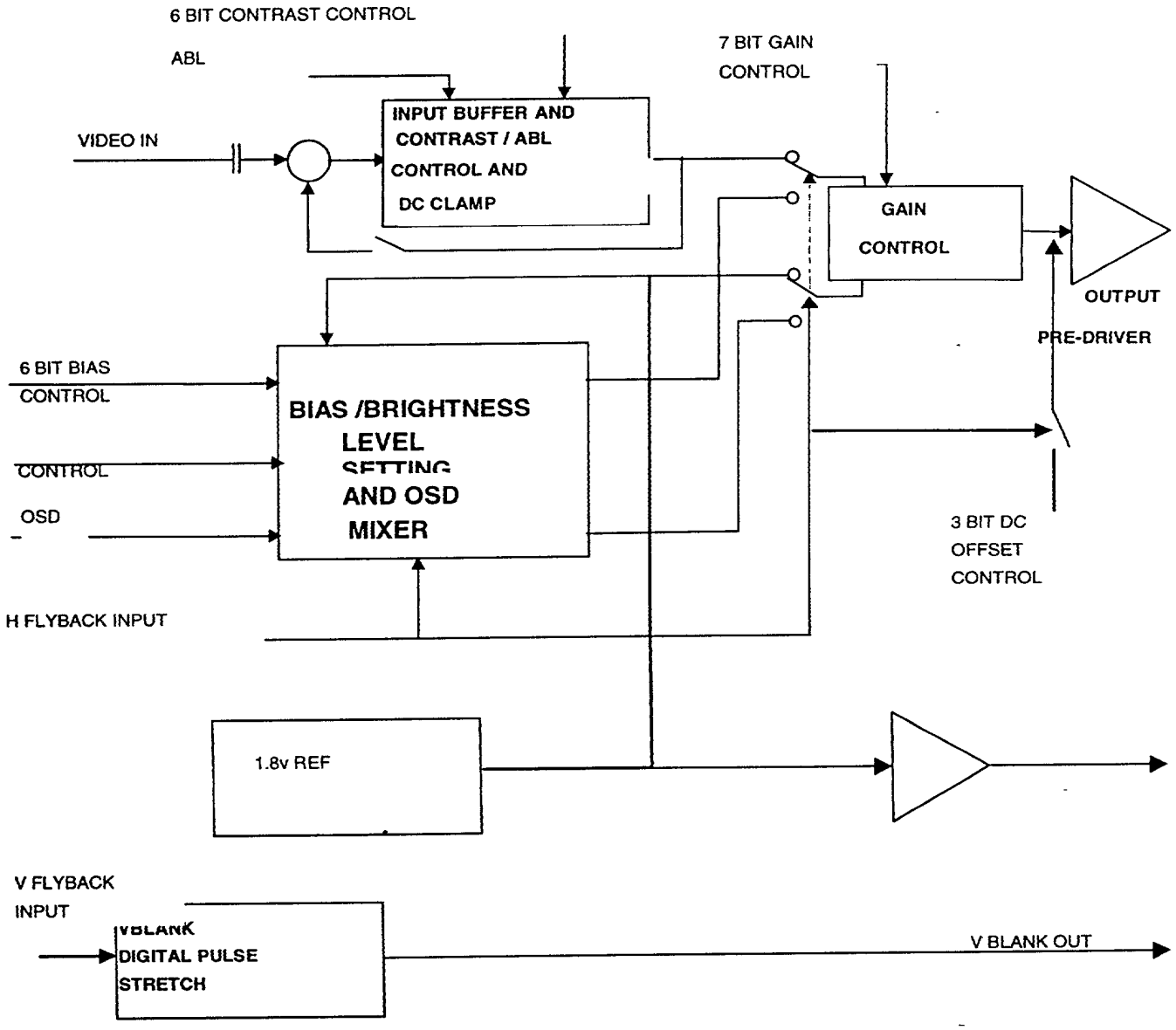

Figure 1 LM1253 PRE-AMP BLOCK DIAGRAM

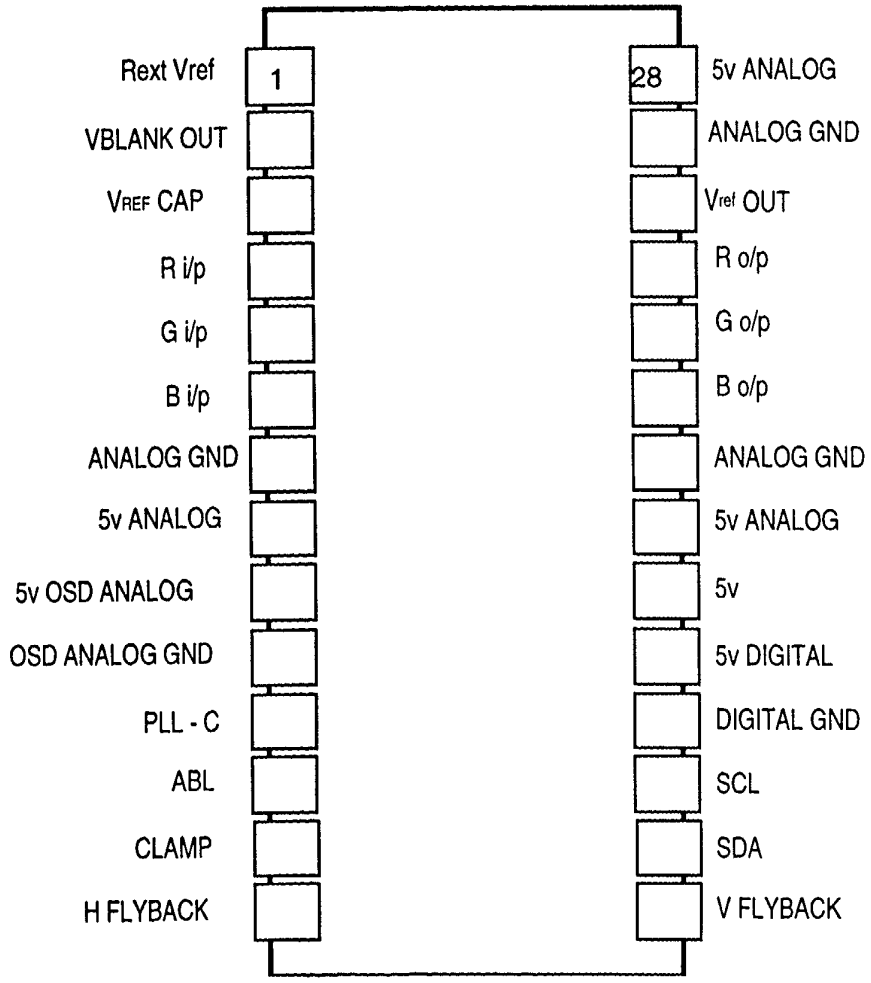

Figure 2 TOP VIEW (FINAL PIN OUT TO BE DETERMINED)

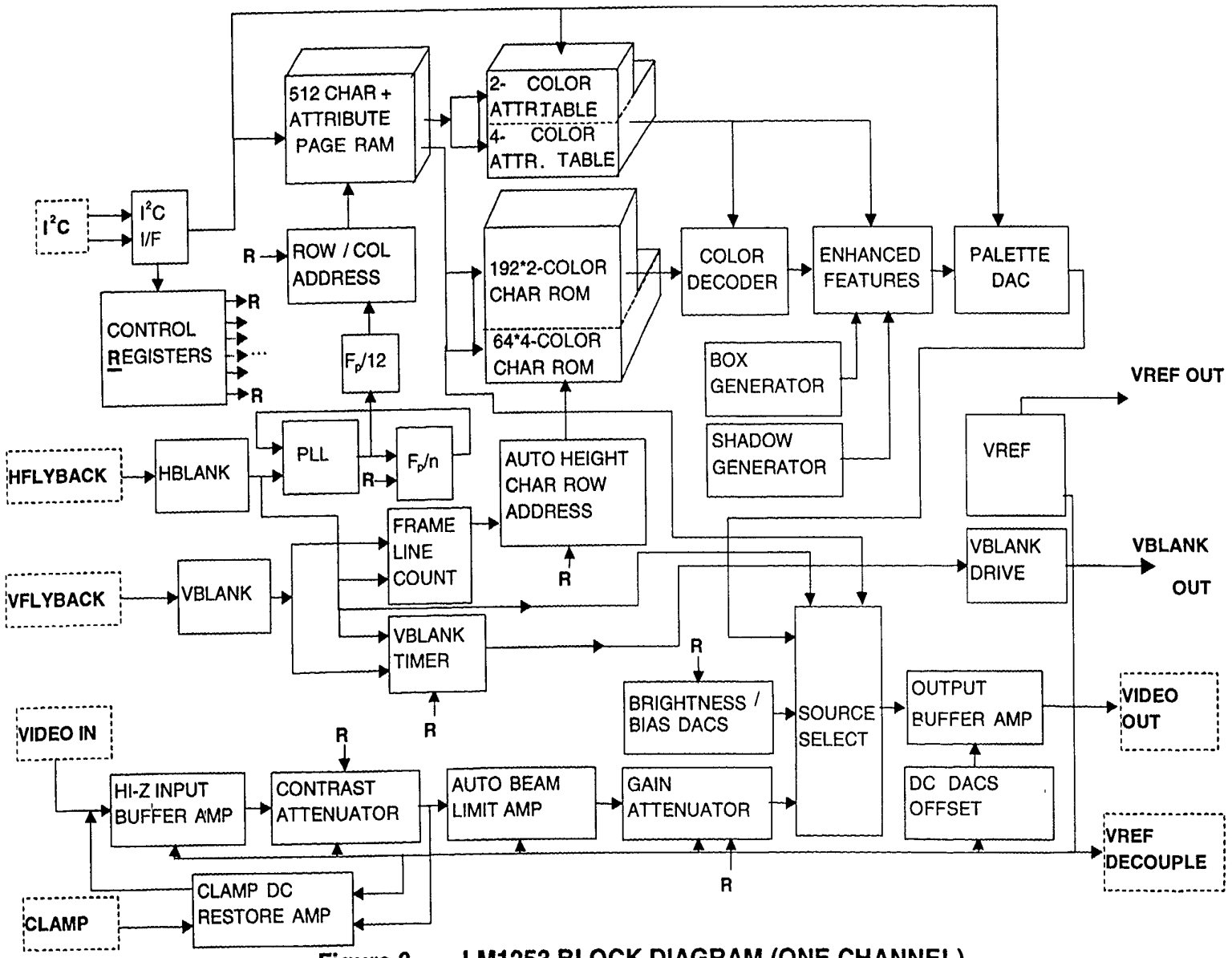

Figure 3 LM1253 BLOCK DIAGRAM (ONE CHANNEL)

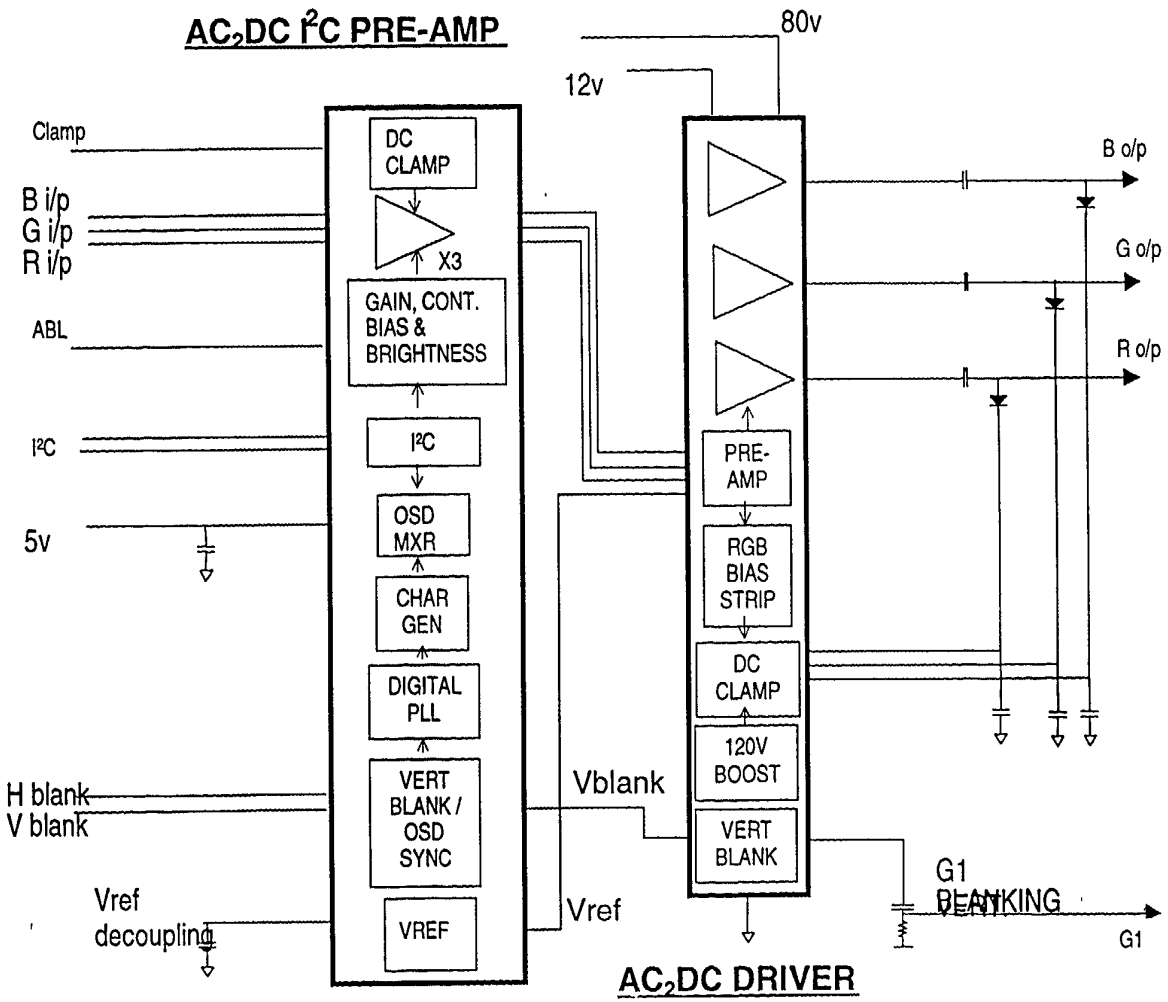

Figure 4 SIMPLIFIED SCHEMATIC DIAGRAM

1.4 SPECIAL FEATURES

The AC_2DC ™ system using the National Videoplex ™ multiplexed video signal to send the video signal and DC clamp level from preamplifier to driver. The basic signal scheme is shown in the figure below.

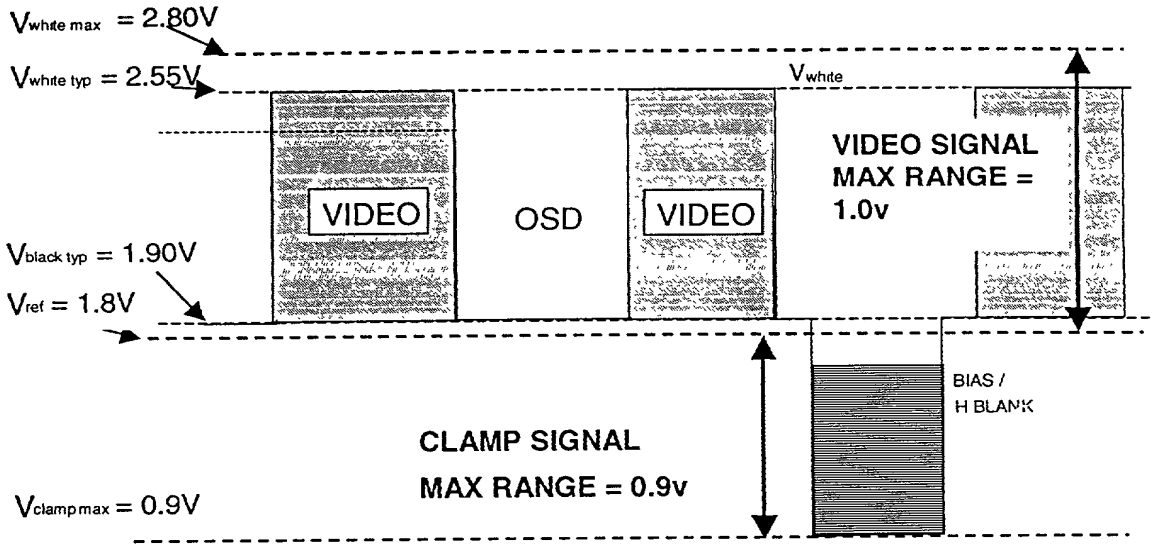

Figure 5 AC_2DC™ SYSTEM VIDEOPLEX™ VIDEO SIGNAL

The response to the video and clamp amplifiers to the Videoplex ™ signal is shown in the figure below.

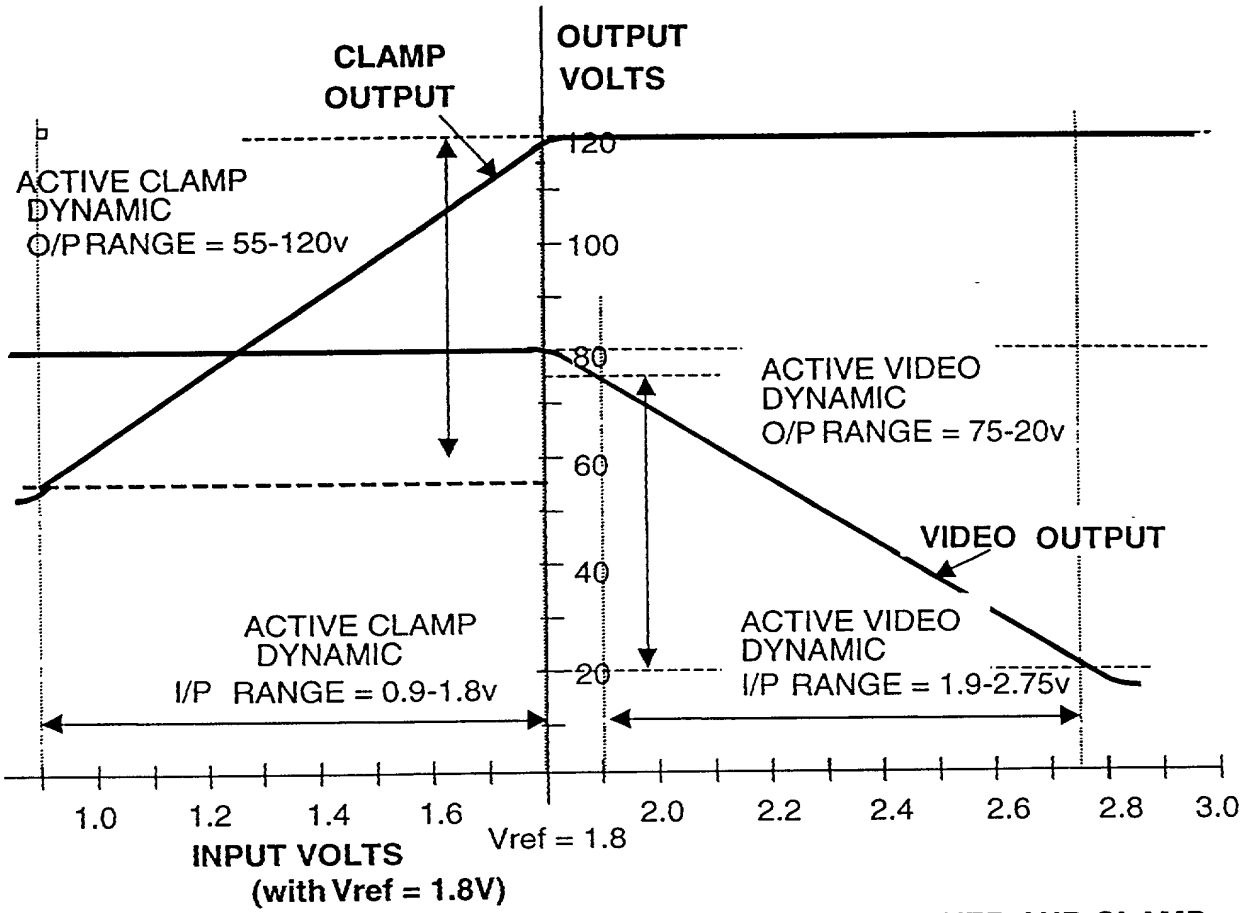

Figure 6 DC I/O TRANSFER CHARACTERISTIC FOR DRIVER AND CLAMP AMPLIFIERS

(Test Conditions: V_{ref} = 1.8v, Vcc1 = 80v, Vcc2 = 120v, Vbb = 12v)

1.5 ACTIVE VIDEO TRANSFER CHARACTERISTIC

The nominal value of the active signal at the output shall vary according to the following law:

$$V_O = \{ [(CONT + 6.93) / 69.3] * [(GAIN + 29.6) / 92.6] * 1.5 * V_{IN} \} + V_{REF} + \{DC * 0.3/ 7 \}$$

Where:

V_O is the output signal level

V_{IN} is the input signal level before the AC coupling

V_{REF} is the reference signal level

CONT is the Contrast register value (0-63)

GAIN is the Contrast register value (0-63)

DC is the DC register value (0-7)

From this it can be seen that the contrast control range is 20dB (10X) and the gain control range is 10dB (3.2X). The DC offset can vary the active video DC output level by 300mV in total, allowing a total range of adjustment of about 19.5V in eight 2.4V steps at the output of a typical AC_2DC^{TM} CRT driver.

The contrast and gain changes will operate immediately with changes in DAC value, as there is no filtering of the DAC outputs.

1.6 OSD TRANSFER CHARACTERISTIC

The nominal value of the OSD signal at the output shall vary according to the following law:

$$V_{O\text{-}OSD} = V_{OSD} * \{(GAIN + 29.6) / 92.6\} + V_{REF} + \{DC * 0.3/ 7\}$$

Where:

$V_{O\text{-}OSD}$ is the output signal level during OSD

V_{OSD} is the internal OSD signal level from the OSD palette generator

V_{REF} is the reference signal level

GAIN is the Contrast register value (0-63)

DC is the DC register value (0-7)

From this it can be seen that the OSD is not affected by the Brightness control, but is proportion to the Gain control, with a gain control range of 10dB (3.2X). The DC offset will affect the OSD output level by 300mV in total.

In order to provide smooth control of the video, all output parameters affected by digital controls must vary monotonically and smoothly, without any visible artifacts or glitches perceptible in the CRT image during adjustment.

NOTE: There should be no measurable variation in OSD level at the output with variations in bias or brightness control registers or contrast control register values, or with video input level.

1.7 OSD BRIGHTNESS / BIAS TRANSFER CHARACTERISTIC

The nominal value of the brightness / bias portion of the signal at the output during blanking shall vary according to the following law:

$$V_O = V_{REF} - \{BIAS * 0.50 / 63\} - \{ (\{BRIGHTNESS-31\} * 0.20 / 63) * [(GAIN + 29.6) / 92.6] \} - \{ PEDESTAL * 0.2 / 7\}$$

Where :

V_O is the output signal level during the blanking period

V_{REF} is the reference signal level

BIAS is the Bias register value (0-63)

BRIGHTNESS is the Brightness register value (0-63)

GAIN is the Contrast register value (0-63)

PEDESTAL is the Pedestal register value (0-7)

From this it can be seen that the bias offset control range subtracts between 0 and 0.35v from the value of V_{REF} during blanking. The bias offset voltage is unaffected by changes in the other controls.

The brightness control range is bi-directional and adds or subtracts an additional amount between –0.2v and +0.2v from the value of V_{REF} during blanking, when gain is set between 0 and 63. This corresponds to a maximum brightness control range of about +/-14V at the CRT cathode.

The pedestal register controls the offset to the brightness control, in order that bi-direction operation of the brightness control is always possible at all bias voltage settings.

If gain is reduced, the brightness output voltage is reduced in proportion to allow gain tracking of the brightness control.

In order to provide smooth control of the video, all output parameters affected by digital controls must vary monotonically and smoothly, without any visible artifacts or glitches perceptible in the CRT image during adjustment.

NOTE 1: There should be no measurable variation in blanking level at the output with variations in contrast control register values, or with video input level.

1.8 INTERNAL INTERFACE REQUIREMENTS

1.8.1 OSD SIGNAL

The pre-amp interfaces internally with the OSD and I^2C digital control circuitry. This part of the IC is defined in section 2 of this document.

The digital and analog portions of the IC have separate external ground and Vcc connections and suitable layout considerations must be made to prevent digital noise from interfering in any way with the analog portion of the IC and vice versa.

The OSD signals are provided in analog format and originate within a 3 bit pallet DAC control block, which sets the amplitude depending upon the palette selected and the setting of the OSD I^2C controlled contrast level.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$V_{OSDHIGH\ MAX}$	Typical Maximum OSD high level	Pallete set at max. OSD level Max		V_{ref} + 1v		V
$V_{OSDHIGH\ MIN}$	Typical OSD black level	Pallete set at max. OSD level Max		V_{ref}		V

1.8.2 OSD CROSSTALK:

Special care must be taken in the design of the analog switches that select between OSD and normal video in order to ensure that any cross talk between the video and the

OSD is within the specified limits. This may require double attenuation switches such as shown conceptually below in to achieve the limits required in the specification table.

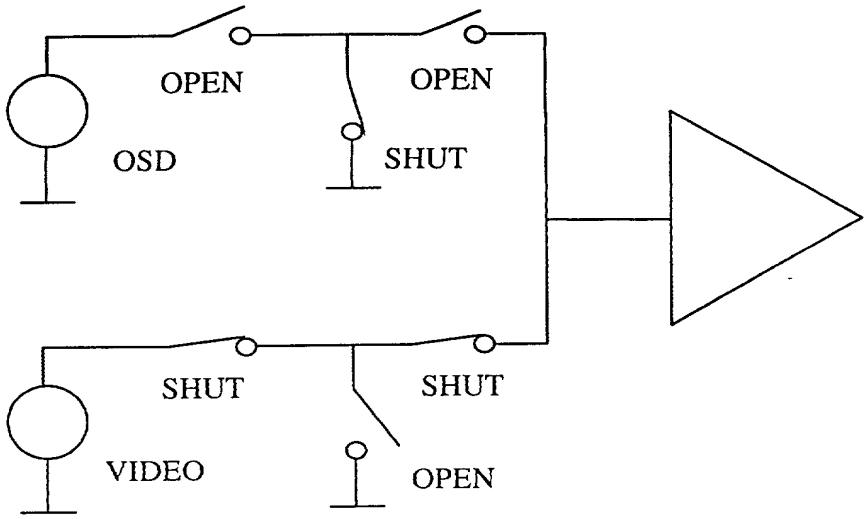

Figure 7 DOUBLE SWITCHED OSD /VIDEO SOURCES FOR MINIMUM CROSSTALK

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1.9 EXTERNAL INTERFACE REQUIREMENTS

1.9.1 ABL CONTROL INPUT

The Auto Beam Limit control reduces the gain of the video amplifier in response to a control voltage proportional to the CRT beam current. This is required for CRT life and X-ray protection. The beam current limit circuit application is as shown in the figure below: when no current is being drawn by the EHT supply, current flows from the supply rail through the ABL resistor and into the ABL input of the IC. The IC clamps the input voltage to a low impedance voltage source.

When current is drawn from the EHT supply, the current passes through the ABL resistor, and reduces the current flowing into the ABL input of the IC.

When the EHT current is high enough, the current flowing into the ABL input of the IC drops to zero. This current level determines the ABL threshold and is given by:

$$I_{ABL} = \frac{V_S - V_{ABL\,TH}}{R_{ABL}}$$

Where:

V_S is the external supply (usually the CRT driver supply rail (ie 80v)

$V_{ABL\,TH}$ is the threshold ABL voltage of the IC

R_{ABL} is the ABL resistor value

I_{ABL} is the ABL limit

When the voltage on the ABL input drops below the ABL threshold of the pre-amp, the gain of the pre-amp reduces, which reduces the beam current. A feedback loop is thus established which acts to prevent the average beam current exceeding I_{ABL}.

The ABL input of the amplifier must act like a low impedance clamp to a constant voltage source while sinking current. When the ABL voltage drops below the threshold level, then the ABL input must appear as a very high impedance input, with negligible input bias current.

The ABL has two ranges of operation: over the initial range of approximately -5dB, the transfer characteristic of the preamplifier remains linear. This is sufficient for normal operation. Beyond –5dB of attenuation, the additional –5dB attenuation may result in some degradation of the linearity or frequency response of the LM1253.

Note that temperature drift characteristics while ABL is active (ie not at maximum gain) is not important, as the ABL control loop operates to maintain constant beam current.

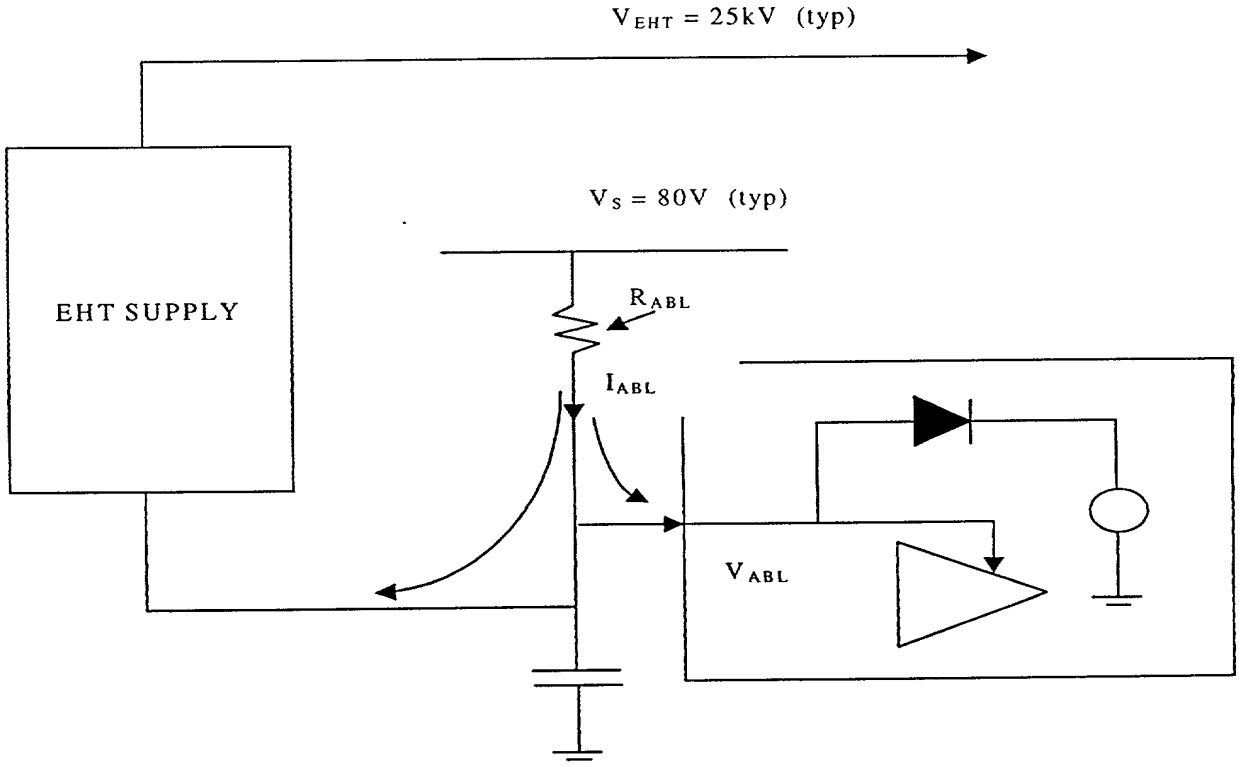

Figure 8 BASIC ABL CIRCUIT

1.9.2 INPUT SIGNAL AC COUPLING

The input AC coupling capacitors also serve as the DC clamp control capacitors. The value is important as it forms part of a switched DC control loop. It is also very important that the input source resistance is kept low, in order to prevent video content dependant offsets appearing.

1.9.3 VERTICAL BLANKING

A negative active vertical blanking signal is provided by the LM1253. The signal is a logic signal. The leading edge of the vertical blanking signal is set by the VFLYBACK waveform, and the width of the pulse is set by the Vertical Blank Duration Control Register.

1.9.4 VREF OUTPUT

The LM1253 provides a stable 1.8v reference voltage that can be used by the driver and clamp circuit in the AC_2DC^{TM} system.

1.10 SPECIFICATION REQUIREMENTS

1.10.1 LIMITS OF ABSOLUTE MAXIMUM RATINGS (NOTES 1 & 3)

The following parameters will be specified in the data sheet; the specification limits of the device should be within the range specified below:

5v Voltage, V_{CC} Equal to or better than +6 V

Input Voltage, V_{IN} Equal to or better than -0.5 V to Vcc + 0.5 V

Storage Temperature Range, T_{STG} Equal to or better than -65 °C to +150 °C

Lead Temperature (Soldering, <10 sec.) Equal to or better than 300 °C

ESD Tolerance, Human Body Model Equal to or better than 2kV min

ESD Tolerance, Machine Model Equal to or better than 200V min

Limits of Operating Ranges (Note 2)

V_{CC} Equal to or better than +4.5 V to + 5.5V

T_{jmax} Equal to or better than +150C

1.10.2 DESIGN FOR ROBUSTNESS

The AC_2DC^{TM} pre-amp will incorporate full ESD protection.

1.10.3 AC PREAMP ELECTRICAL CHARACTERISTIC TARGETS AND LIMITS

Unless otherwise noted: V_{CC} = +5 V, V_{IN} = 0.7VAC, C_L = 8 pF, Video signal output = 1 V_{PP} at 1 MHz, T_C = 50 °C, V_{ref} =1.80v, V_{ABL} = V_{CC} (See the figure below for Test Circuit)

ACTIVE VIDEO SIGNAL PARAMETER TEST SETTINGS:

Test setting control values (unless other wise stated):

CONTROL:	NO. OF BITS	BASIC TEST SETTING 1	BASIC TEST SETTING 2	BASIC TEST SETTING 3	BASIC TEST SETTING 4
CONTRAST	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MAX (Hex 3F)
R,G,B GAIN	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	Set for 1v p-p on all channels
BRIGHTNESS	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)
R,G,B, BIAS	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)
VIDEO DC OFFSET	3	MIN (Hex 00)	MIN (Hex 00)	MAX (Hex 07)	MIN (Hex 00)

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable

ACTIVE VIDEO SIGNAL PARAMETER SPECIFICATIONS:

The following parameters apply to the active video portion of the waveform.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
I_{CC1MAX}	Maximum Supply Current	Test Setting (1), Per Channel, No Output Load		250		mA
$V_{OUT\ BLK\ TYP}$	Typical Active Video Black level Output Voltage	Test Setting (1), No AC Input Signal,		V_{ref}		V_{DC}
$V_{OUT\ WHITE\ TYP}$	Typical Active Video White level Max Output Voltage	Test Setting (4), AC Input Signal,		2.7		V
t_{rtyp}	Typical Rise Time	Note 5, 10% to 90%, Test Setting (4), AC Input Signal,		2.7		nS
t_{ftyp}	Typical Fall Time	Note 5, 90% to 10%, Test Setting (4), AC Input Signal,		2.7		nS
$A_{CONTRAST}$	Contrast Max-Min Adjustment range	Test Setting (3), AC Input Signal,		20		dB
A_{GAIN}	Gain Max-Min Adjustment range	Test Setting (3), AC Input Signal,		10		dB
$A_{MAX\ TYP}$	Typical max signal Voltage Gain	Test Setting (3), AC Input Signal,		1.5		V/V
$V_{ABL\ TH}$	Auto Beam Limit Control upper limit	Note 6, Test Setting (4), AC Input Signal,		TBD_{ABL}		V
$V_{ABL\ RANGE}$	Auto Beam Limit Control Voltage Range	Note 6, Test Setting (4), AC Input Signal,		2		V
ΔA_{ABL}	Auto Beam Limit Control range	Note 6, Test Setting (4), AC Input Signal		- 10		dB
$V_{ABL\ CLAMP\ MAX}$	Maximum Auto Beam Limit Input voltage during clamping	Note 6, Test Setting (4), AC Input Signal, $I_{ABL} = I_{ABL\ MAX}$		V_{CC}		V
LE_{ABL}	ABL Linearity Error	Test Setting (4), Triangular signal input source (see note 4), For setting of the ABL voltage between 0 to –5dB attenuation		5%		%

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$t_{PW\ CLAMP}$	Minimum clamp pulse width		200			ns
$V_{CLAMP\ MAX}$	Maximum low level clamp pulse voltage		1			V
$V_{CLAMP\ MIN}$	Minimum high level clamp pulse voltage		2.2		2.5	V
$V_{VBLANK\ HIGH}$	Minimum high level of vertical blank output	$V_{VREF\ BLANK} < 0.75V$	V_{REF} +1			V
$V_{VBLANK\ LOW}$	Minimum output voltage of V_{VBLANK} pin during Vertical blank	$I_{VBLANK\ OUT}$ = 100uA			V_{REF}-1	V
$t_{V\ BLANK}$	Typical vertical blanking Rise or Fall Time				1	uS
$t_{V\ BLANK-STRT\ PROP}$	Typical maximum vertical blanking start propagation delay	Reference $V_{VFLYBACK}$ input			200	ns
C_{IP}	Input AC coupling capacitor	Test Setting (4)			TBD	nF
R_{IP}	Minimum Typical Input resistance	Test Setting (4)		20		Meg Ohm
	Thermal Smear	Tested in Monitor with NSC Neck Board and AC_2DC^{TM} Driver			None Visible	
V_{ref}	Typical Vref ouput voltage		1.75	1.8	1.85	V
V_{ref} I_{max}	Maximum operational sourced output current of V_{ref}		300	NA	NA	uA

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Linearity Error is the variation in step height of a 16 step staircase input signal waveform with 0.7vp-p level at the input, subdivided into 16 equal steps, with each step approximately 100ns in width.

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Note 5: Input from signal generator: t_r, t_f < 1 nS.

Note 6: ABL should provide smooth decrease in gain over the operational range of 0db to –5db

$$\Delta A_{ABL} = A(V_{ABL} = V_{ABL\ MAX\ GAIN}) - A\ (V_{ABL} = V_{ABL\ MIN\ GAIN})$$

Beyond –5db the gain characteristics, linearity and pulse response may depart from normal values.

1.10.4 BRIGHTNESS/BIAS SIGNAL PARAMETER TEST SETTINGS

The following specification parameters apply to the test of the brightness / bias portion of the waveform.

Test setting control values (unless other wise stated):

CONTROL:	NO. OF BITS	BASIC TEST SETTING 5	BASIC TEST SETTING 6	BASIC TEST SETTING 7	BASIC TEST SETTING 8
CONTRAST	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)
R,G,B GAIN	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MAX (Hex 3F)
BRIGHTNESS	6	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)	MIN (Hex 00)
R,G,B, BIAS	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MIN (Hex 00)
VIDEO DC OFFSET	3	MIN (Hex 00)	MIN (Hex 00)	MIN (Hex 00)	MIN (Hex 00)
PEDESTAL OFFSET	3	MAX (Hex 07)	MAX (Hex 07))	MAX (Hex 07)	MIN (Hex 00)

1.10.5 BRIGHTNESS/BIAS SIGNAL PARAMETER SPECIFICATIONS:

The following parameters apply to the brightness /bias portion of the output waveform.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$V_{BLANK\ MAX\ TYP}$	Typical Maximum blanking level	Test Setting (5)		V_{REF} - 0.90		V
$V_{BLANK\ MIN}$	Minimum blanking level	Test Setting (8)		V_{REF}		V
$t_{BLK\ rtyp}$	Typical Blanking Rise Time	Test Setting (5), 10% to 90%,		30		nS
$t_{BLK\ ftyp}$	Typical Blanking Fall Time	Test Setting (5), 10% to 90%,		30		nS

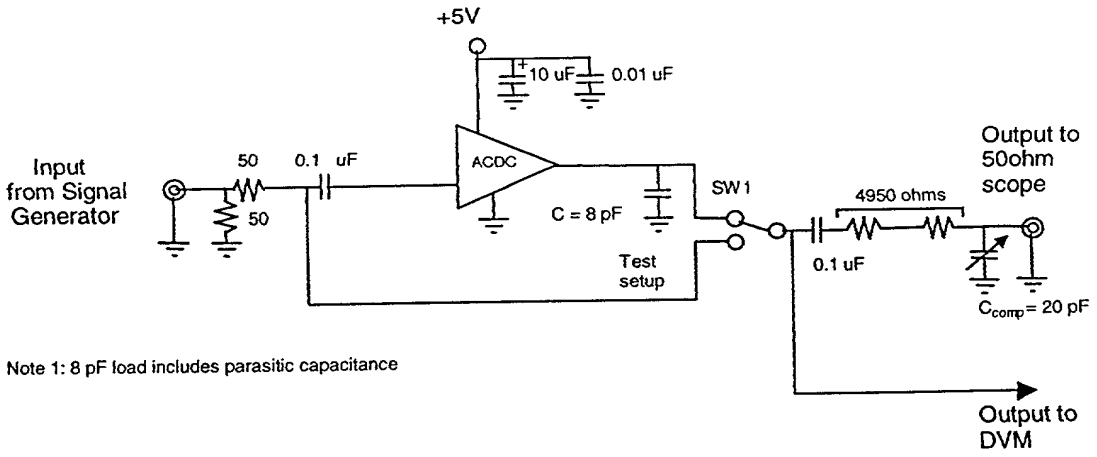


Figure 9 TEST CIRCUIT (ONE CHANNEL)

The above figure shows a typical test circuit for evaluation of the LM1253 preamp. This circuit is designed to allow testing of the AC_2DC ™ preamp in a 50-ohm environment without the use of an expensive FET probe. The 4950 ohm resistor at the output forms a 100:1 voltage divider when connected to a 50 ohm load. Ccomp must be adjusted for flat response with SW1 in test setup position.

2 ANALOG/DIGITAL INTERFACE

2.1 OSD VIDEO DAC

2.1.1 OSD DAC BASIC OPERATION

The OSD DAC is controlled by the 9 bit (3x9bits) OSD video information coming from the pixel serializer register (see also section 1 and section 3).

The OSD DAC is shown conceptually in the figure below, where the gain is programmable by the 2bit OSD CONTRAST register, in 4 stages to give the required peak OSD signal as specified in section 1.

The OSD DACs uses the internal reference voltage, V_{ref} .

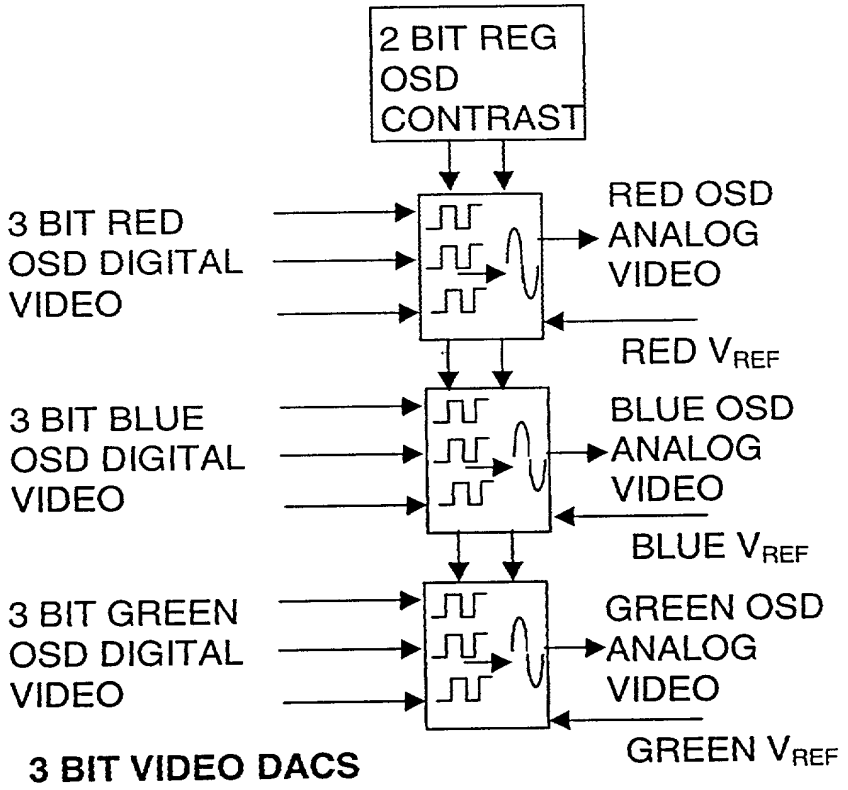


Figure 10 BLOCK DIAGRAM OF OSD DACS

The OSD DAC creates the analog signal biased with respect to the reference voltage. The DAC must be monotonic and linear. The full scale ouput voltage with an OSD video input of '111' and a maximum contrast setting of '11' should be nominally 1v.

2.2 ANALOG / DIGITAL EXTERNAL INTERFACE SIGNALS

These signals are presented to the digital section of the IC at the external interface to the monitor system via the device pins:

2.2.1 HFLYBACK:

HFLYBACK is an analog signal input from the monitor horizontal scan. .HBLANK is digital signal derived from the horizontal flyback pulse shaped as per the figure below:

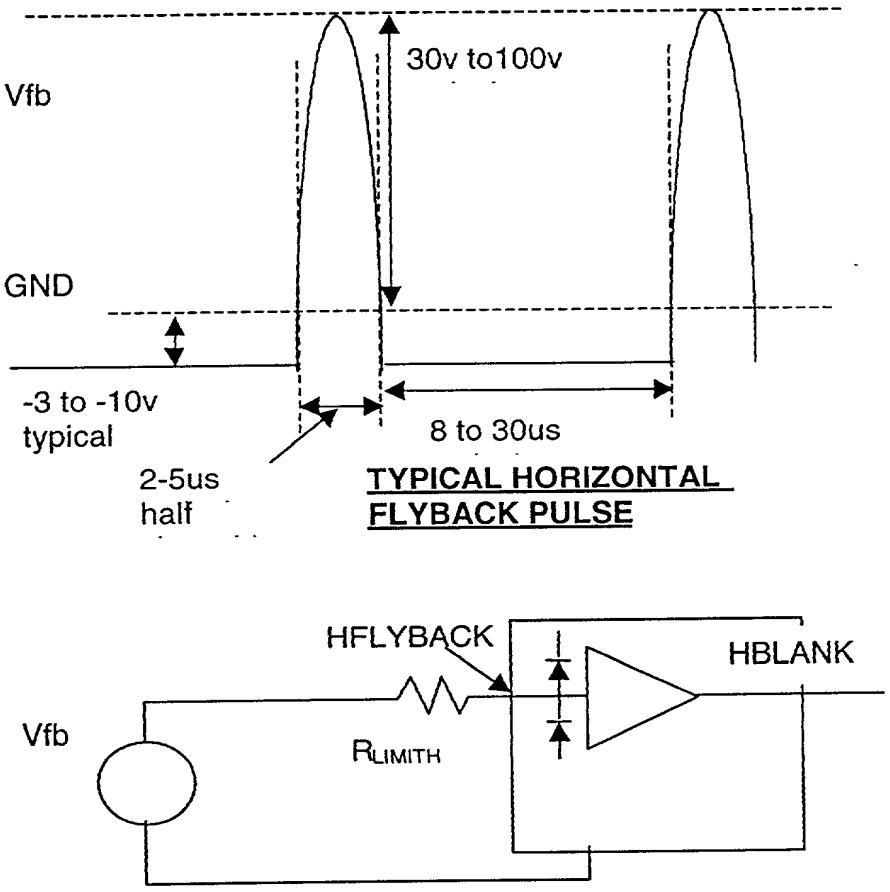


Figure 11 HFLYBACK INPUT PULSE

R_{LIMITH} is set to limit the input current into the IC to a maximum value of +2mA during flyback and –150uA during normal forward scan. The internal input impedance of the I/O (R_{HFIN}) is low to limit the maximum voltage swing at the input to within the supply rail and ground. The IC interface circuit creates a digital signal from this waveform, which is used as the blanking signal, and termed HBLANK. This signal is used by the video amplifier for blanking the video, and by the OSD generator as the horizontal sync reference for the PLL.

The PLL will detect if no signal is present at the input for any sustained period. When no signal is present, the PLL will produce a signal to set the video output level to the black level.

R_{LIMITH} shall be as large as possible (nominally 100kohm).

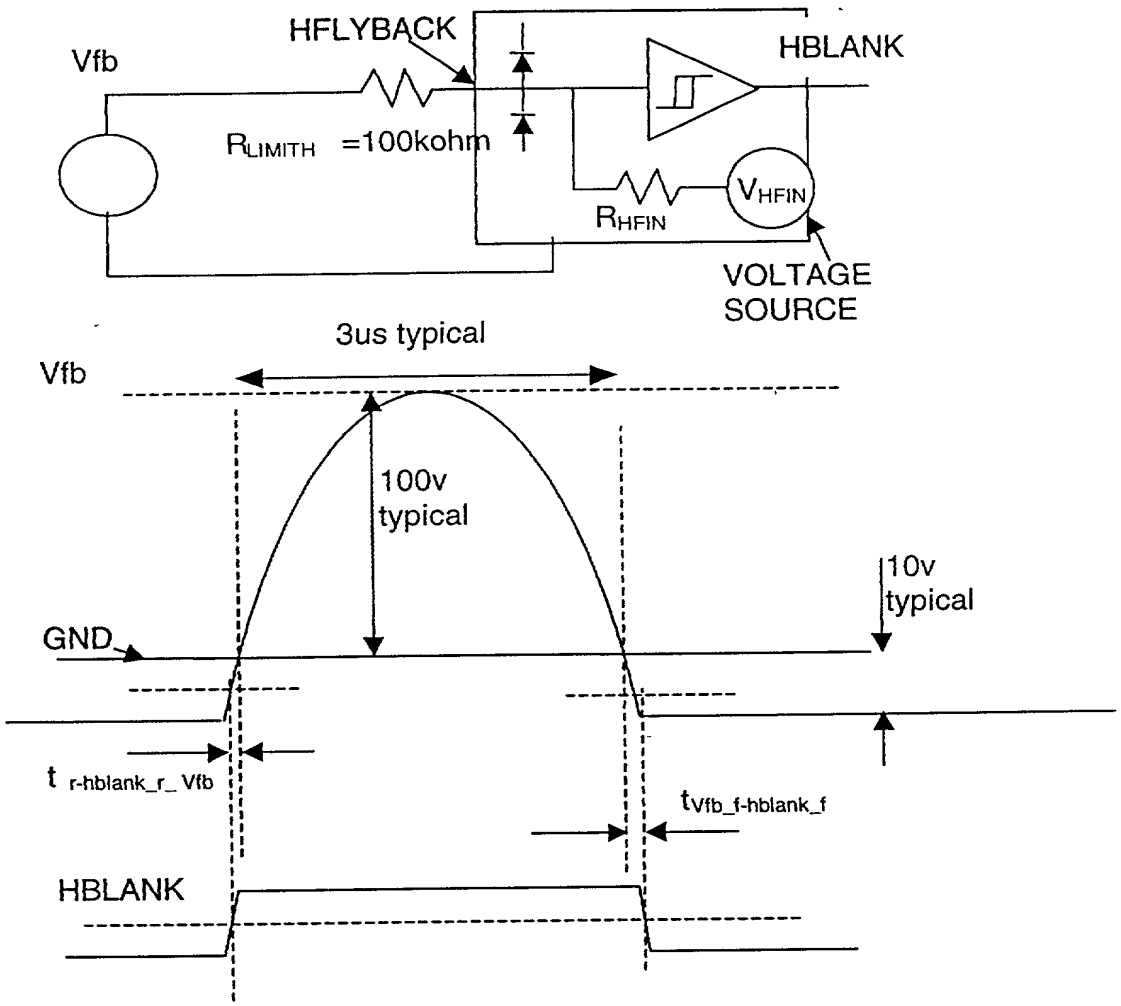


Figure 12 TEST CONDITIONS FOR HBLANK SIGNAL

The input should have voltage excursion clamps to prevent the input being damaged by excessive input voltage swing. The HBLANK line should normally trigger high when the rising edge of the flyback pulse has passed through the AC zero level. It should

normally trigger low within 100ns of the flyback signal falling below the AC zero volt level.

PARAMETER	SYMBOL	MIN	TARGET	MAX
HBLANK rising edge to Flyback signal rising edge zero crossing point	$t_{r\text{-}hblank_r_Vfb}$			
Flyback signal falling edge zero crossing point to HBLANK falling edge	$t_{Vfb_f\text{-}hblank_f}$		0	
I_{OUT} HBLANK detection threshold	I_{TH}		-20uA	
Minimum normal forward scan current at lowest horizontal frequency that will ensure HBLANK signal will activate normally	$I_{IN\text{-}MIN}$		-30uA	
Maximum normal forward scan current at lowest horizontal frequency that input can withstand	$I_{IN\text{-}MAX}$		TBD	
Maximum flyback scan current @ 125kHz that input can withstand	I_{IN+MAX}		TBD	

2.2.2 VFLYBACK:

This is an analog signal from the monitor vertical scan. The analog waveform is AC coupled if necessary to remove the low frequency and DC components. This signal is fed to the input of the IC via a current limiting resistor to prevent the positive and negative excursions of the signal causing excessive current or voltage swing at the input to the IC.

R_{LIMITV} is set to limit the maximum input voltage swing into the IC to less than the supply rails. The input stage is a voltage source V_{VFIN} with an input resistance of R_{VFIN}. The input to the IC is positive edge triggered, and ignores the falling edge. Because of horizontal rate noise on the waveform, the input buffer incorporates hysteresis, triggering at a positive going threshold of V_{VTH+} and a negative going threshold of V_{VTH-}. The input should have very low bias current (<50uA) due to the high source impedance, and should have ESD clamps to prevent the input being damaged by excessive input voltage swing.

The input buffer produces a digital signal VSTART which is used to start the VBLANK timer. The positive rising edge of VSTART sets a counter timer, which counts horizontal periods using the HBLANK signal. The timer resets VBLANK when it reaches the value preset in the register VCOUNT (set by the micro-controller over I^2C).

While the output VBLANK is active, an AND function prevents any further transitions on the VSTART waveform from retriggering the counter.

The positive edge of the VSTART signal is initially transmitted through to VBLANK through an OR function, as the timer may take up to one horizontal line period to begin timing the duration of the pulse. The application must ensure that the VFLYBACK vertical flyback pulse is kept high during that initial period to prevent the output VBLANK from switching between high and low states.

The end of the VBLANK pulse should not dither between lines (causing 1line vertical jumping) due to slight variations in the phase of VFLYBACK and HBLANK.

05/25/00 15:39:39 "LM1253"

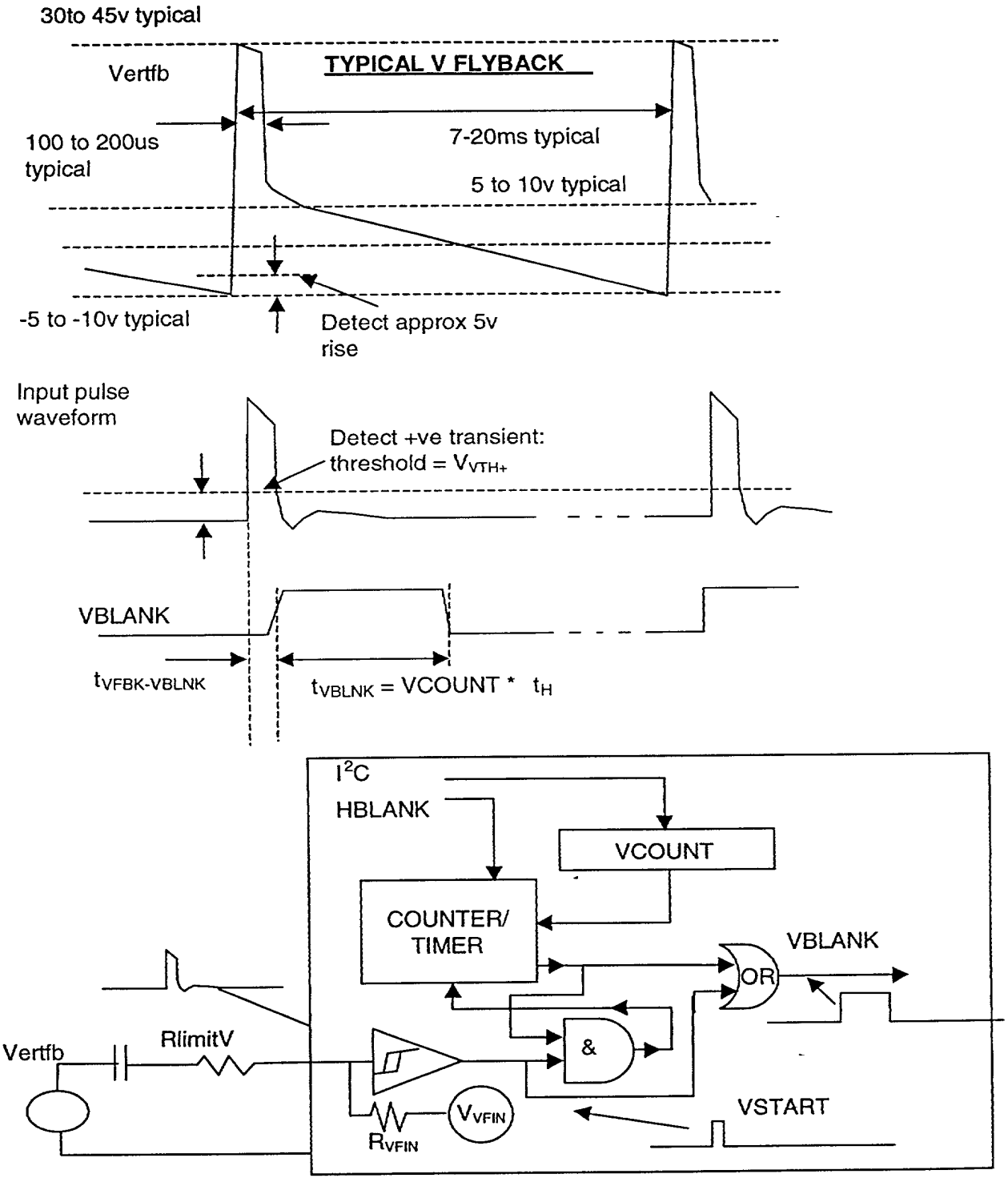


Figure 13 VERTICAL FLYBACK INPUT PULSE

PARAMETER	SYMBOL	MIN	TARGET	MAX
Vertical flyback signal rising edge to VBLANK rising edge	$t_{Vfb_r-hblank_r}$		<1us	
VBLANK duration	t_{VBLNK}		(VCOUNT) $*t_H$	
VFLYBACK input voltage source	V_{VFIN}		0.25* Vcc	
VFLYBACK input voltage source resistance	R_{VFIN}		8k	
VFLYBACK positive going detection threshold	V_{VTH+}		V_{VFIN} + 500mV	
VFLYBACK negative going detection threshold	V_{VTH-}		V_{VFIN} + 150mV	

2.2.3 LOSS OF VERTICAL FLYBACK PULSE

Loss of vertical flyback pulse implies that the monitor is not scanning, and therefore no image is being displayed. The HBLANK and VBLANK pulses are still required by the AC_2DC ™ driver in order to maintain correct bias conditions in the CRT until the power supplies are switched off, but video should be set at black level to prevent front of screen problems.

Loss of vertical flyback will be detected when the frame line counter runs past the previously stored frame line count, N_{FRAME} by more than two lines. The two lines allows for some error in the counting of the number of lines in the frame due to noise on the VFLYBACK pulse.

Note also that interlace mode is supported by the LM1253. In interlace mode, a frame is composed of two sequential fields. In the first field, the odd lines are displayed. In the second field the even lines are displayed. A complete frame consists of an odd number of horizontal lines, so that each field contains a half line. This will result in an alternate half line phase difference between each field of the VFLYBACK pulse with respect to the HBLANK pulse.

Note that the blanking circuit will only detect the absence of a vertical flyback pulse. In that case it will free run at a period of $N_{FRAME}*t_H$. It will not reliably detect or blank the video if an erratic pulse occurs.

Examples of the operation of the VBLANK signal are shown below. Note: the change from one vertical frequency to another is sometimes continuous, with no break in VFLYBACK pulses.

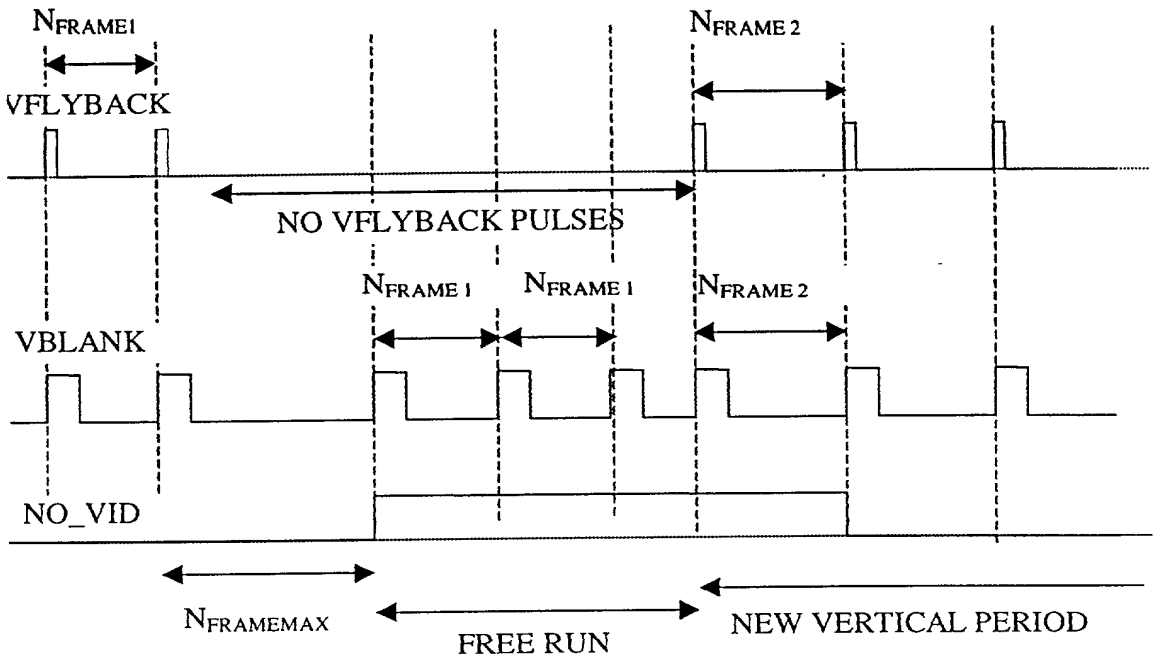


Figure 14 EXAMPLE1: OPERATION WHEN FRAME PERIOD CHANGES FROM N_{FRAME1} TO N_{FRAME2}

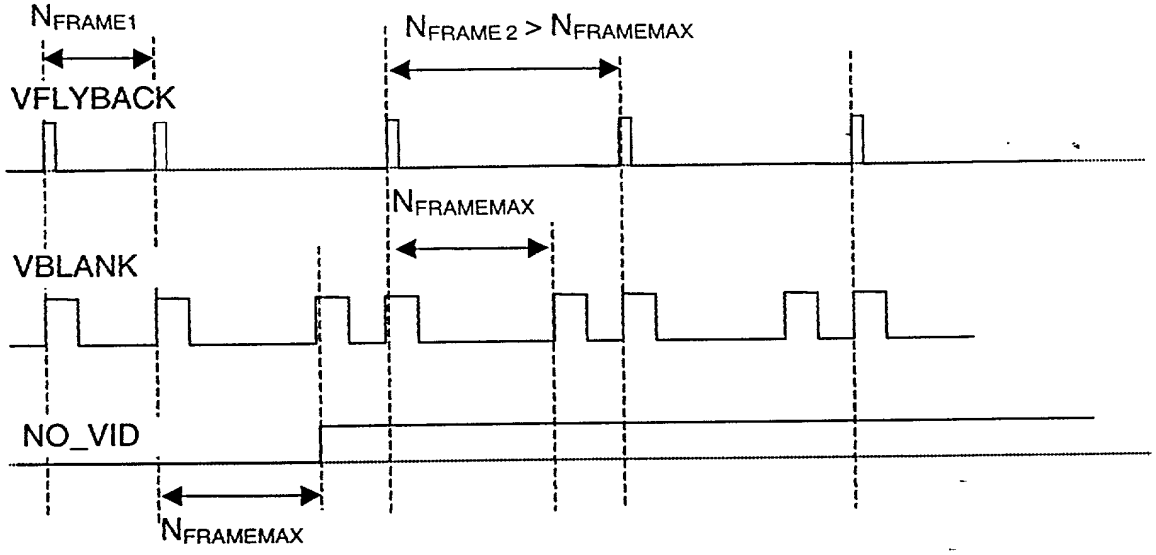


Figure 15 EXAMPLE2: OPERATION WHEN FRAME PERIOD CHANGES FROM N_{FRAME1} TO N_{FRAME2}, WHERE $N_{FRAME2} > N_{FRAMEMAX}$

2.3 HORIZONTAL PHASE LOCKED LOOP

2.3.1 LOSS OF HORIZONTAL FLYBACK PULSE

Loss of horizontal flyback pulse implies that the monitor is not scanning, and therefore no image is being displayed. The HBLANK pulse is still required by the AC_2DC^{TM} driver in order to maintain correct bias conditions in the CRT until the power supplies are switched off, but video should be set at black level to prevent front of screen problems.

In the absence of an externally supplied horizontal flyback pulse, the PLL will free run and generate its own HBLANK pulse at a frequency of F_{FREE_RUN} after a number of missed horizontal line periods, N_{MISSED}. The PLL free run pulse will be gated into the HBLANK line to the pre-amp to allow normal operation of the pre-amp and driver biasing. The free run pulse width will be between 1/8 and $1/16^{th}$ of the horizontal period.

PARAMETER	SYMBOL	MIN	MAX
HORIZONTAL PERIOD	t_H	20kHz	125kHz
NO. OF PIXELS PER LINE	N_H	HCOUNT	HCOUNT+32
PIXEL CLOCK FREQUENCY	F_P	6.4MHz	96MHz
JITTER	t_{JITTER}	-	0.025% of t_H
DRIFT	dF_{DRIFT}	-	2%
FREE RUN HBLANK FREQUENCY	F_{FREE_RUN}	30kHz	60kHz
MISSING H PERIODS BEFORE FREE RUN FREQUENCY	N_{MISSED}		10
MAXIMUM CAPTURE AND SETTLING TIME IN NUMBER OF H PERIODS AFTER CHANGE IN H FREQUENCY	N_{SETTLE}	0	512

The PLL clock frequency will drift by no more than dF_{DRIFT} over the device operating temperature range.

2.4 VCC DETECT:

The Vcc power supply will be continuously monitored. Should the Vcc supply drop to less the Vcc_{DET} then the LM1253 will set the output video to V_{REF}.

The device should continue to operate down to Vcc_{DET}, although some parameters may fall outside of specification when the supply drops below Vcc_{MIN}.

PARAMETER	SYMBOL	MIN	MAX
Vcc undervoltage detection threshold	Vcc_{DET}	4.0V	4.25V

00720f1 - 03/30/99 09:05:50

3 OSD GENERATOR

3.1 OSD GENERATOR OPERATION

3.1.1 PAGE OPERATION

The block diagram of the OSD generator is shown in the figure below:

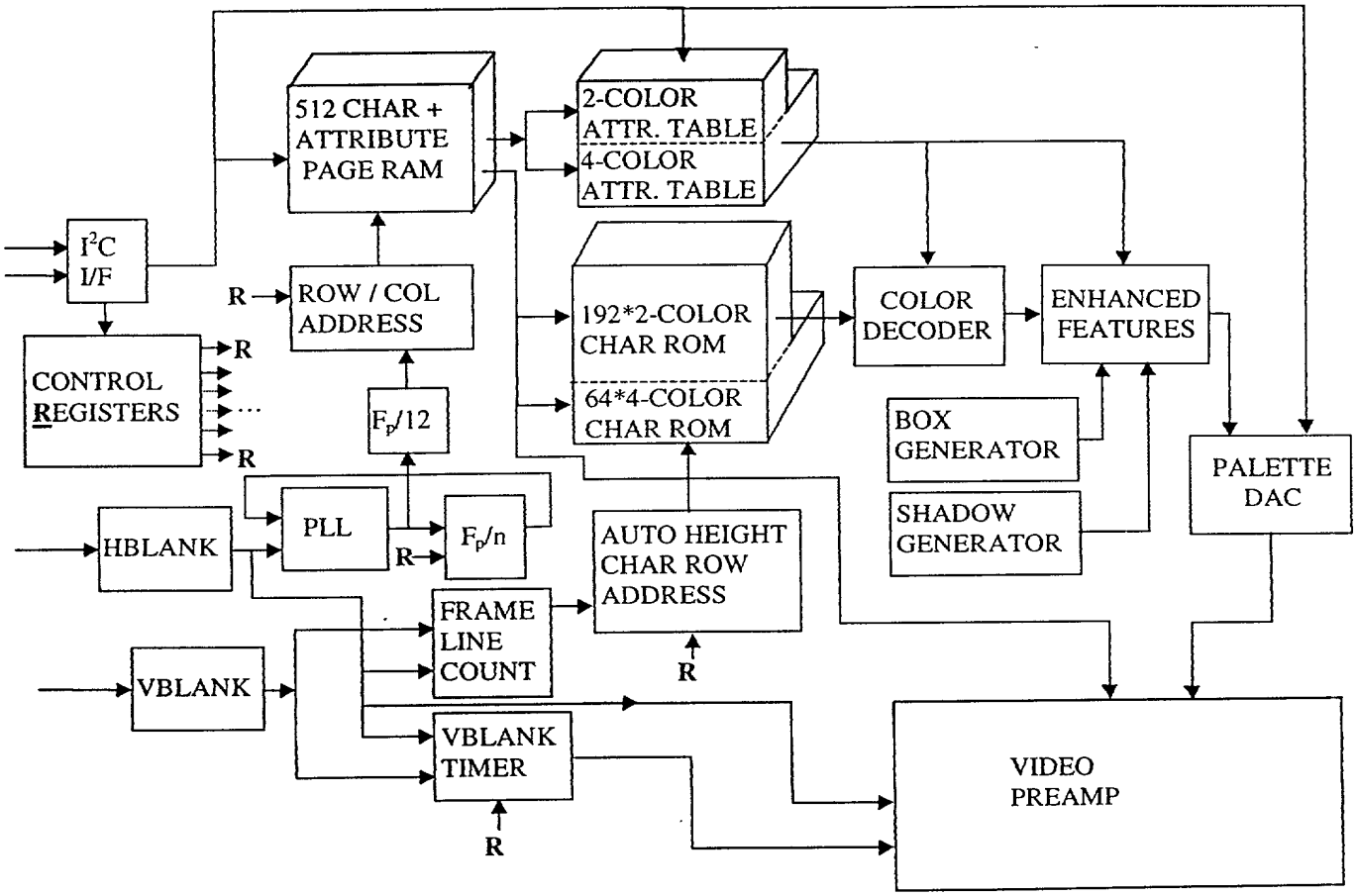


Figure 16 BLOCK DIAGRAM OF THE OSD GENERATOR

Video information is created using any of the 256 pre-defined characters stored in the mask programmed ROM. Each character has a unique 8 bit code that is used as its address. Consecutive rows of characters make up the displayed window. These characters can be stored in the page RAM, written under I^2C controlled commands by the monitor micro-controller. Each row can contain any number of characters up to the limit of the displayable line length, although some restrictions concerning the enhanced features apply on character rows longer than 32 characters.

The number of characters across the width and height of the page can be varied under I^2C control, but the total number of characters that can be stored and displayed on the

screen is limited to 512 including any character row end characters. The horizontal and vertical start position can also be programmed under I^2C control.

3.1.2 WINDOWS

Two separate windows can be opened, utilizing the data stored in the page RAM. Each window has its own horizontal and vertical start position, although the second window should be horizontally spaced at least two character spaces away from the first window.

3.1.3 CHARACTER CELL

Each character is defined as a 12 wide by 18 high matrix of picture elements, or 'pixels'. There are two types of characters defined in the character ROM:

i. **Two-color:** there are 192 two-color characters. Each pixel of these characters is defined by a single bit value. If the bit value is 0, then the color is defined as 'Color 1' or the 'background' color. If the bit value is 1, then the color is defined as 'Color 2', or the 'foreground' color. An example of a character is shown in the figure below:

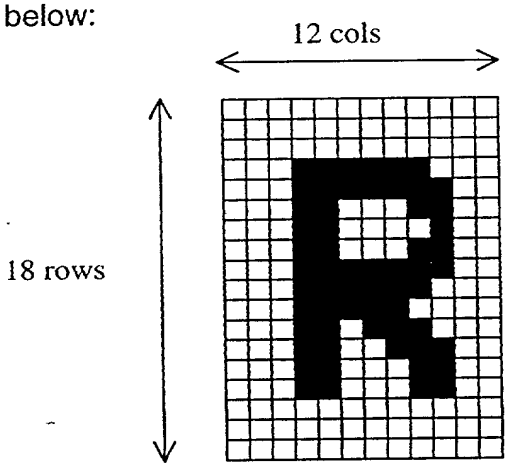


Figure 17 A TWO-COLOR CHARACTER

ii. **Four-color**: there are 64 four-color characters stored in the character ROM. Each pixel of the four-color character is defined by two bits of information, and thus can define four different colors, Color1, Color2, Color3, Color4. Color 1 is defined as the 'back ground' color. All other colors are considered 'foreground' colors, although for most purposes, any of the four colors may be used in any way. Because each four-color character has two bits, the matrix has two planes of ROM.

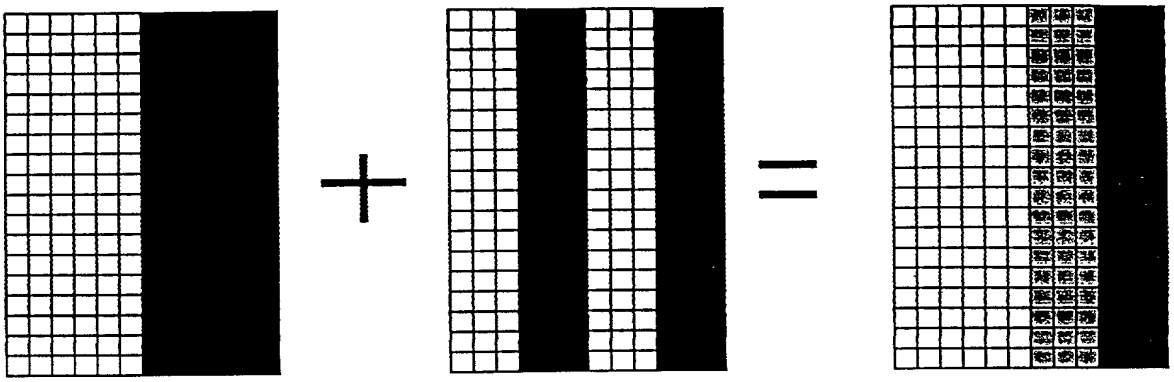


Figure 18 A FOUR COLOR CHARACTER

3.1.4 ATTRIBUTE TABLES

Each character has an attribute value assigned to it in the page RAM. The attribute value is 4 bits wide, making each character entry in the page RAM 12 bits wide in total. The attribute value acts as an address which points to one of 16 entries in either the two-color attribute table RAM or the four-color attribute table RAM. The attribute word in the table contains the coding information which defines which color is represented by color1 and color2 in the two color attribute table and color1, color2, color3, color4 in the four-color attribute table. Each color is defined by a 9bit value, with 3bits assigned to each channel of RGB. A dynamic look up table defines each of the 16 different color combination selections or 'palettes'. As the look up table can be dynamically coded by the micro-controller over the I^2C interface, each color can be assigned to any one of 2^9 (i.e. 512) choices. This allows a maximum of 64 different colors to be used within one page using the 4-color characters, with up to 4 different colors within any one character. and 32 different colors using the 2-color characters, with 2 different colors within any one character.

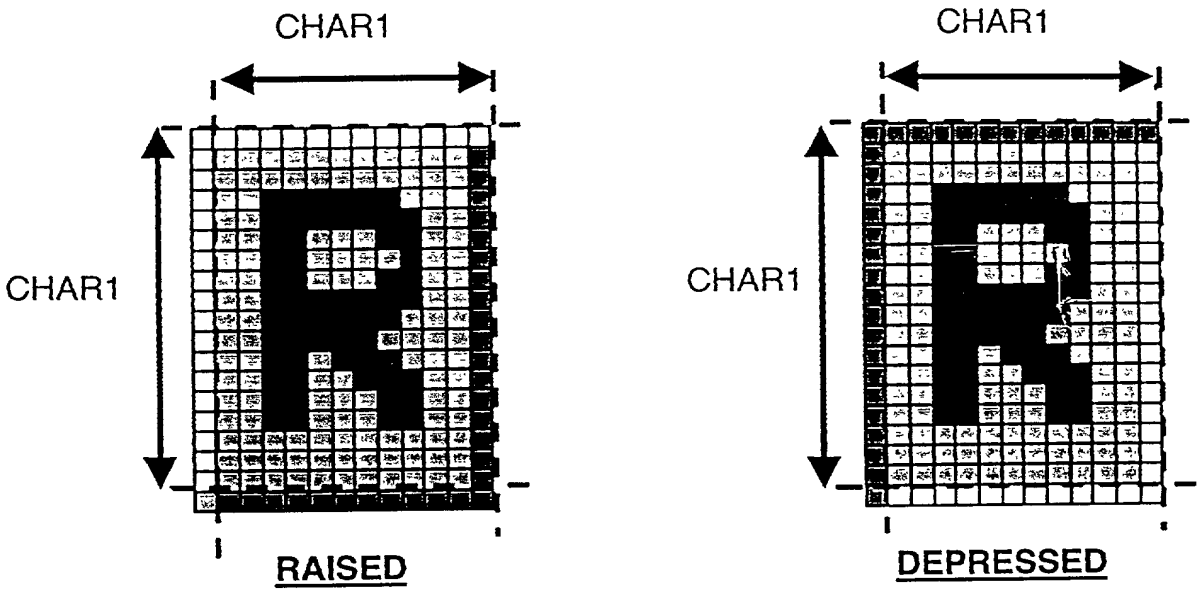
3.1.5 TRANSPARENT DISABLE

In addition to the 9 lines of video data, a tenth data line is generated by the transparent disable bit. When this line is activated, the black color code will be translated as 'transparent' or invisible. This allows the video information from the PC system to be visible on the screen when this is present. Note that this feature is only enabled on Color 1 of the first 8 attribute table entries, in order to allow some black color palettes to be used in combination with the transparent feature.

3.1.6 ENHANCED FEATURES

In addition to the wide selection of colors for each character, additional character features can be selected on character by character basis.

i. Windows95™ style button boxes. The OSD generator examines the character string being displayed and if the 'button box' attributes have been set in the Enhanced feature byte, then a box creator selectively substitutes the character pixels in either or both the top and left most pixel line or column with a button box pixel.



Effect on the screen:

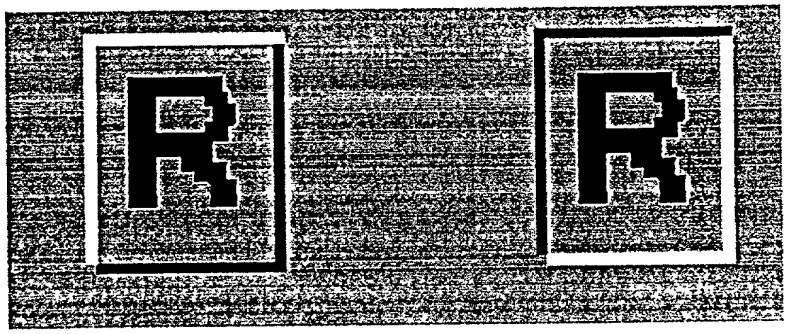


Figure 19 WINDOWS95™ STYLE 'BUTTON BOXES'

The shade of the button box pixel depends upon whether a 'depressed' or 'raised' box is required, and can be programmed by I^2C.The raised pixel color ('highlight') is defined by the value in the color palette register, EF1 (normally white). The depressed pixel ('lowlight') color by the value in the color palette register EF2 (normally gray).

ii. Heavy Button Boxes
When heavy button boxes are selected, the color palette value stored in register EF3 is used for the depressed ('lowlight') pixel color instead of the value in register EF2.

iii. Shadowing: shadowing can be added to two-color characters by choosing the appropriate attribute value for the character. When a character is shadowed, a shadow pixel is added to the lower right edges of the color2 image, as shown in the figure below:

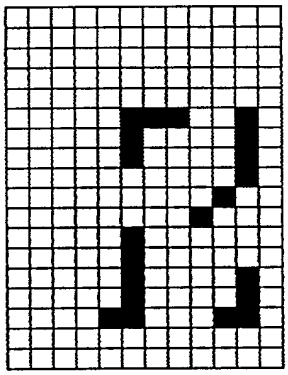


Figure 20 SHADOWING

The color of the shadow is determined by the value in the color palette register EF3 (normally black).

iv. Bordering: a border can be added to the two-color characters. When a character is bordered, a border pixel is added at every horizontal, vertical or diagonal transition between color1 and color2.

005687 35 - 10270

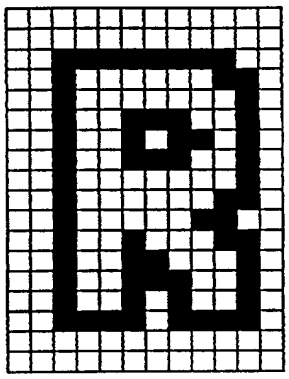


Figure 21 BORDERING

The color of the border is determined by the value in the color palette register EF3 (normally black).

v. Blinking: if blinking is enabled as an attribute, all colors within the character except the button box pixels which have been over-written will alternately switch to color1 and then back to the correct color at a rate determined by the micro-controller under I^2C control.

3.2 MICRO-CONTROLLER INTERFACE

The micro-controller interfaces to the AC/DC Pre-Amp via an I^2C interface. The protocol of the interface begins with a Start Pulse followed by a seven bit Slave Device Address and a Read/Write bit. Each I^2C Slave Device decodes its own address and responds to all reads and writes to that address. The address associated with the AC/DC Pre-Amp is *TBD*.

The figures below show a write and read sequence across the I2C interface.

3.2.1 WRITE SEQUENCE

Following the Start Pulse, the Slave Device Address, the Read/Write bit (a zero, indicating a write) and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit.

The next 8-bits will be the write data associated with the address indicated by the two address bytes. Subsequent write data bytes will correspond to the next increment address locations

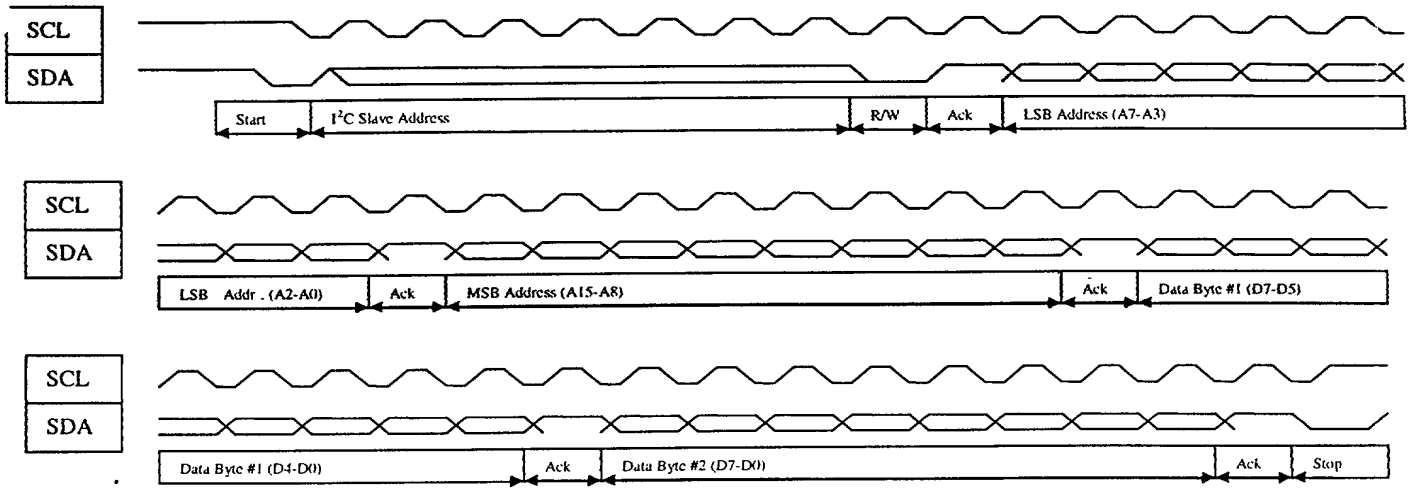


Figure 22 I²C WRITE SEQUENCE

3.2.2 READ SEQUENCE

Read sequences are comprised of two I2C transfer sequences: The first being a write sequence that only transfers the two byte address to be accessed. The second being a read sequence that starts at the address transferred in the previous address only write access and incrementing to the next address upon every data byte read.

The following timing diagram illustrates an entire read sequence:

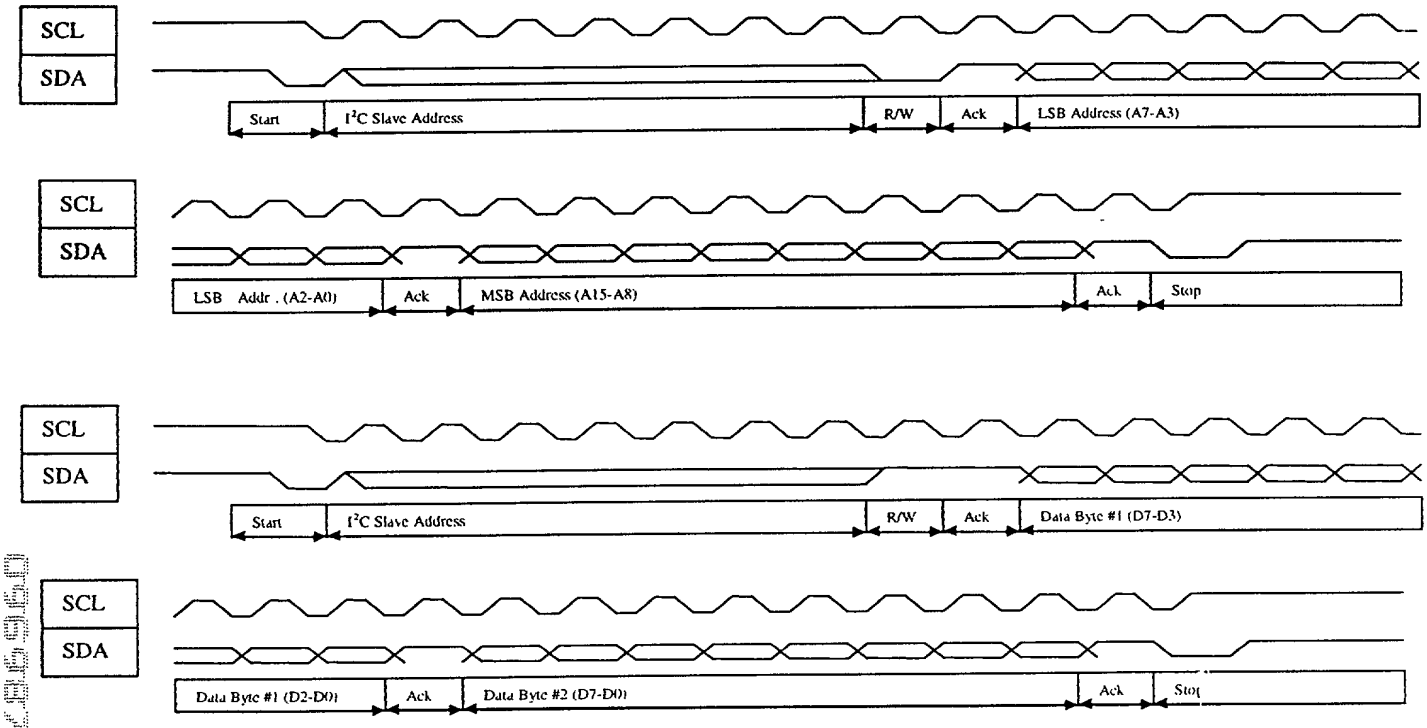


Figure 23 I²C READ SEQUENCE

Following the Start Pulse, the Slave Device Address, the Read/Write bit (a zero, indicating a write) and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access.

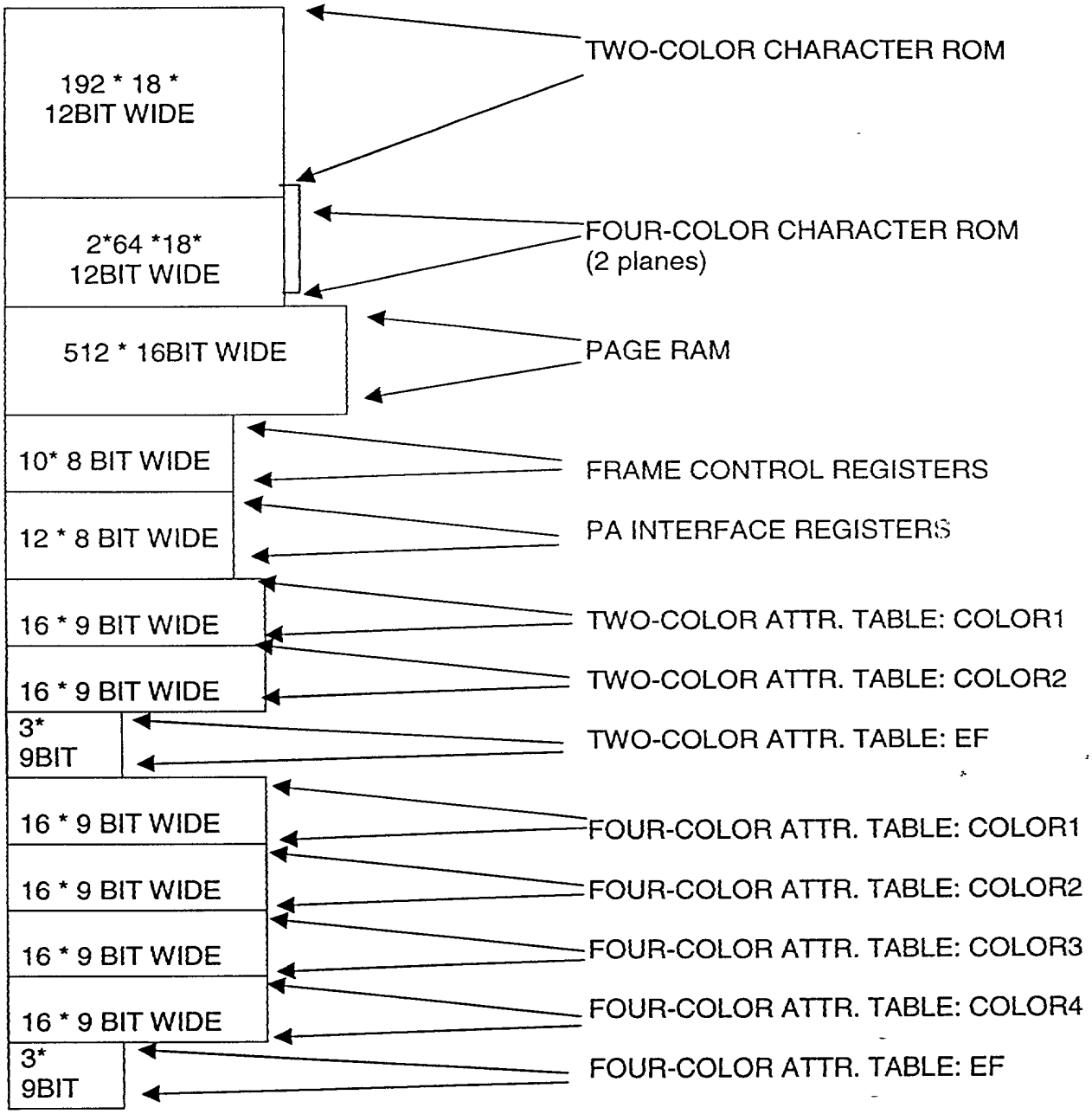
Next the read data access will be performed beginning with the Start Pulse, the Slave Device Address, the Read/Write bit (a one, indicating a read) and the Acknowledge bit; Then the next 8-bits will be the read data driven out by the AC/DC Pre-Amp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations.

3.3 I²C IC ADDRESS

The slave address of the LM1253 is 5D.

3.4 I²C AC/DC PRE-AMP ADDRESS MAP

3.4.1 ROM, RAM AND REGISTERS ADDRESSED BY I²C



3.4.2 CHARACTER ROM

Address Range	R/W	Description
0000h – 2FFFh	R	ROM Character Fonts, 192 two-color Character Fonts that are Read-Only. The format of the address is as follows: A15-A14: Always zeros. A13-A6: Character value (00h – BFh are valid values) A5-A1: Row of the character (00h-11h are valid values) A0: Low byte of line when a zero. High byte of line when a one. The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data Bits 7-4 are "don't cares". Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line.
3000h – 3FFFh	R	ROM Character Fonts, 64 four-color Character Fonts that are Read-Only. The format of the address is as follows: A15-A14: Always zeros. A13-A6: Character value (C0h – FFh are valid values) A5-A1: Row of the character (00h-11h are valid values) A0: Low byte of line when a zero. High byte of line when a one. The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data Bits 7-4 are "don't cares". Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line. NOTE: The value of Bit 0 of the Character Font Access Control Register (I2C Address 8402h) is a zero, it indicates that the Bit 0 data value of the four-color pixels is being accessed via these addresses. When the value of Bit 0 of the Access Control Register is a one, it indicates that the Bit 1 data value of the four-color pixel is being accessed via these addresses.
4000h – 7FFFh		RESERVED.

3.4.3 DISPLAY PAGE RAM

Address Range	R/W	Description
8000h – 81FF	R/W	Display Page RAM Characters. A total of 512 display characters, skipped line, end-of-row and end-of-window character codes may be supported via this range. To support skipped lines and character attributes a number of special case rules are used when writing to this range. (Refer to the Display Page RAM section of this document for more details.)

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3.4.4 PRE-AMP INTERFACE REGISTERS

LM1253 OSD Interface Registers										
Register	Address	Reset	D7	D6	D5	D4	D3	D2	D1	D0
Fonts-2color	0000-2FFE		PIXEL[7:0]							
	+1						PIXEL[11:8]			
Fonts-4color	3000-3FFE		PIXEL[7:0]							
	+1						PIXEL[11:8]			
Display Page	8000-83FF		CHAR_CODE[7:4] or reserved				CHAR_CODE[3:0] or ATTR_CODE			
FRMCTRL1	8400	10				TD	CDPR	D2E	D1E	OSE
FRMCTRL2	8401	80	PIXELS_PER_LINE[2:0]			BLINK_PERIOD[4:0]				
CHARFONTACC	8402	00							ATTR	FONT4
VBLANKDUR	8403	10	VBLANK_DURATION[6:0]							
CHARHTCTRL	8404	51	CHAR_HEIGHT[7:0]							
BBHLCTRLB0	8405	FF	R[1:0]		B[2:0]		G[2:0]			
BBHLCTRLB1	8406	01								R[2]
BBLLCTRLB0	8407	00	B[2:0]		B[2:0]		G[2:0]			
BBLLCTRLB1	8408	00								R[2]
CHSDWCTRLB0	8409	00	B[2:0]		B[2:0]		G[2:0]			
CHSDWCTRLB1	840A	00								R[2]
reserved	840B	00								
ROMSIGCTRL	840D	00								CRS
ROMSIGDATAB0	840E	00	CRC[7:0]							
ROMSIGDATAB1	840F	00	CRC[15:8]							
HSTRT1	8410	13	HPOS[7:0]							
VSTRT1	8411	14	VPOS[7:0]							
reserved	8412	00								
COLWIDTH1B0	8414	00	COL[7:0]							
COLWIDTH1B1	8415	00	COL[15:8]							
COLWIDTH1B2	8416	00	COL[23:16]							
COLWIDTH1B3	8417	00	COL[31:24]							
HSTRT2	8418	56	HPOS[7:0]							
VSTRT2	8419	5B	VPOS[7:0]							
W2STRTADRL	841A	00	ADDR[7:0]							
W2STRTADRH	841B	01								ADDR[8]
COLWIDTH2B0	841C	00	COL[7:0]							
COLWIDTH2B1	841D	00	COL[15:8]							
COLWIDTH2B2	841E	00	COL[23:16]							
COLWIDTH2B3	841F	00	COL[31:24]							
BISTCONTROL	8420	00							BFAIL	BEN
BISTADDR0	8421	00	ADDR[7:0]							
BISTADDR1	8422	00								ADDR[8]
BISTCOMPARE0	8423	00	COMPARE_DATA[7:0]							
BISTCOMPARE1	8424	00					COMPARE_DATA[11:8]			
BISTREAD0	8425	00	READ_DATA[7:0]							
BISTREAD1	8426	00					READ_DATA[11:8]			

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3.4.5 PRE-AMP INTERFACE REGISTERS

LM1253 Pre-amp Interface Registers									
RGAINCTRL	8430	60	RGAIN[6:0]						
BGAINCTRL	8431	60	BGAIN[6:0]						
GGAINCTRL	8432	60	GGAIN[6:0]						
CONTRCTRL	8433	30	CONTRAST[5:0]						
RBIASCTRL	8434	20	RBIAS[5:0]						
BBIASCTRL	8435	20	BBIAS[5:0]						
GBIASCTRL	8436	20	GBIAS[5:0]						
BRIGHTCTRL	8437	20	BRIGHTNESS[5:0]						
DCOFFSET	8438	94	PEDESTAL[2:0]			OSD_CONT[1:0]		DC_OFFSET[2:0]	
GLOBALCTRL	8439	00						PS	BV
reserved	843A	00							
PLLFREQRNG	843E	16			IVIGAIN[1:0]		IVISTAT[1:0]	PFR[1:0]	
SRTSTCTRL	843F	00	PCT	AID	TEE	MUX[1:0]		BCE	SRST

3.4.6 TWO-COLOR ATTRIBUTE TABLE

LM1253 Two-Color Attribute Registers									
ATT2C0n	8440 + (n*4)		C1R[1:0]		C1B[2:0]		C1G[2:0]		
ATT2C1n	+1		C2R[0]	C2B[2:0]			C2G[2:0]		C1R[2]
ATT2C2n	+2				EF[3:0]			C2R[2:1]	
ATT2C3n	+3								

Two-color display character Attribute Table. The attributes for two-color display characters may be written or read via the following address format:
A15-A6: Always 1000_0100_01b.
A5-A2: Attribute code (0h-Fh are valid values), n
A1-A0: Determines which of the 3 bytes is to be accessed.

NOTE: In the table, n indicates the attribute number 0<=n<=15

NOTE: When writing, bytes 0 through 2 must be written, in that order. Bytes 0 through 2 will take effect after byte 2 is written.

Since byte 3 contains all reserved bits, this byte may be written, but no effect will result.

When reading, it is OK to read only one, two, or all three bytes.

3.4.7 FOUR-COLOR ATTRIBUTE TABLE

LM1253 Four-Color Attribute Registers								
ATT4C0n	8500 +(n*8)		C1R[1:0]		C1B[2:0]		C1G[2:0]	
ATT4C1n	+1		C2R[0]	C2B[2:0]		C2G[2:0]		C1R[2]
ATT4C2n	+2				EF[3:0]			C2R[2:1]
ATT4C3n	+3							
ATT4C4n	+4		C3R[1:0]		C3B[2:0]		C3G[2:0]	
ATT4C5n	+5		C4R[0]	C4B[2:0]		C4G[2:0]		C3R[2]
ATT4C6n	+6							C4R[2:1]
ATT4C7n	+7							

Four-color display character Attribute Table. The attributes for four-color display characters may be written or read via the following address format:
A15-A7: Always 1000_0101_0b
A6-A3: Attribute value (0h-Fh are valid values), n
A2-A0: Determine which of the six bytes of the attribute is to be accessed.

NOTE: In the table, n indicates the attribute number, 0<=n<=15

NOTE: When writing, bytes 0 to 2 must be written, in that order and bytes 4 to 6 must be written, in that order.

Bytes 0 through 2 will take effect after byte 2 is written. Bytes 4 through 6 will take effect after byte 6 is written.

Since bytes 5 and 7 contain all reserved bits, these bytes may be written, but no effect will result.

When reading, it is OK to read only one, two, or all three bytes.

3.5 DISPLAY PAGE RAM

3.5.1 THE OSD WINDOW

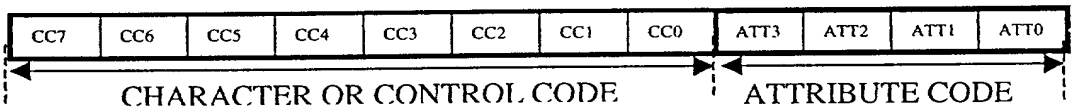
The Display Page RAM contains all of the 8 bit display character codes and their associated 4 bit attribute codes, and the special 12 bit page control codes - the row-end, skip-line parameters and window-end characters.

The LM1253 has a distinct advantage over many OSD generators that it allows variable size and format windows. The window size is not dictated by a fixed geometry area of RAM. Instead, 512 locations of 12 bit words are allocated in RAM for the definition of the windows, with special control codes to define the window size and shape.

Window width can be any length supported by the number of pixels per line that is selected divided by the number of pixels in a character line. It must be remembered that OSD characters displayed during the monitor blanking time will not be displayed on the screen, so the practical limit to the number of horizontal characters on a line is reduced by the number of characters within the horizontal blanking period.

3.5.2 CHARACTER CODE AND ATTRIBUTE CODE

Each of the 512 x12 bit locations in the page RAM is comprised of an 8 bit character or control code, and a 4 bit attribute code:



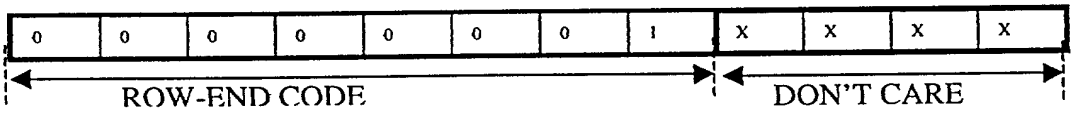
Bits 11-4 Character Code: These 8 bits define which of the 254 characters is to be called from the character ROM. Valid character codes are 02h –FFh.

Bits 3-0: Attribute code. These 4 bits address the attribute table used to specify which of the 16 locations in RAM specify the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, the other for 4-color characters.

Each of the characters are stored in sequence in the page RAM. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') lines to be added between character rows.

3.5.3 ROW END CODE

To signify the end of a row of characters, a special 'Row-End (RE) code is used in place of a character code.



Bits 11-4 Row-End Code: A special character code of 01h

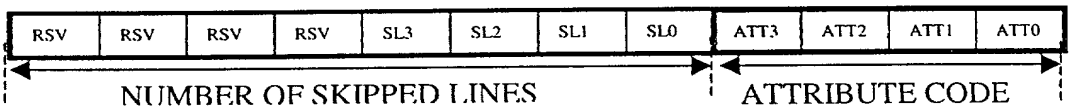
Bits 3-0: Don't care

The RE character tells the OSD generator that the character codes following must be placed on a new row in the displayed window.

3.5.4 SKIPPED LINE PARAMETERS

Each displayed row of characters may have up to 15 skipped (ie blank) lines beneath it in order to allow finer control of the vertical spacing of character rows. (Each skipped line is treated as a single auto-height character pixel line, so multiple scan lines may actually displayed in order to maintain accurate size relative to the character cell).

To specify the number of skipped lines, the first character in each new row of characters to be displayed is interpreted differently than the other characters in the row. Instead of interpreting the data in the location as a character code, the information of the 12 bit word is defined as follows:



Bits 11-8 Reserved.

Bits 7-4: Skipped Lines. These four bits determine how many blank pixel lines will be inserted between the present row of display characters and the next row of display characters. A range of 0-15 may be selected.

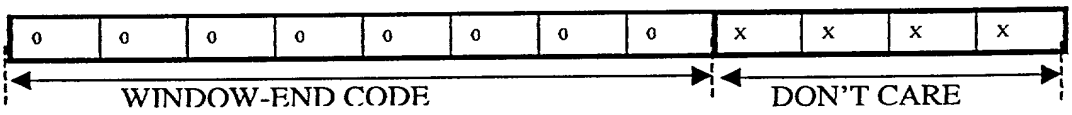
Bits 3-0: Attribute code. The pixels in the skipped lines will normally be Color 1 of the addressed 2-Color Attribute Table entry. Note that the pixels in the first line immediately below the character may be overwritten by the pixel override system that creates the button box. (Refer to the Box Formation Section for more information).

Each new line MUST start with an SL code, even if the number of skipped lines to follow is zero. An SL code MUST always follow an RE control code.

An RE code may follow an SL code if several 'transparent' lines are required between sections of the window (see example 3 below). In this case, skipped lines of zero characters are displayed, causing a break in the window.

3.5.5 WINDOW-END CODE

To signify the end of the window, a special 'Window-End (WE) code is used in place of a Row-End code.



Bits 11-4 Row-End Code: A special character code of 00h

Bits 3-0: Don't care

The WE control code tells the OSD generator that the character codes following belong to another displayed window at the next window location.

A WE control code may follow normal characters or an SL parameter, but never an RE control code.

3.5.6 WRITING TO THE PAGE RAM

The Display Page RAM can contain up to 512 of the above listed characters and control codes. Each character, or control code will consume one of the possible 512 locations. For convenience, a single write instruction to bit 3 of the Frame Control Register (8400h) can reset the page RAM value to all zero.

Display Window 1 will also start at the first location (corresponding to the I^2C address 8000h). This location must always contain the Skip-Line (SL) parameters associated with the first row of Display Window 1. Subsequent locations should contain the characters to be displayed on row 1 of Display Window 1, until the RE character code or WE character code is written into the Display Page-RAM.

The skip-line parameters associated with the next row must always be written to the location immediately after the preceding row's row-end character. The only exception to this rule is when a window-end character (value 00h) is encountered. It is important to note that a row-end character should not precede a window-end character (otherwise the window-end character will be interpreted as the next row's skip-line parameters). Instead, the window-end character will both end the row and the window making it unnecessary to precede it with a row-end character.

The I^2C Format for writing a sequence of display characters is minimized by allowing sequential characters with the same attribute code to send in a string as follows:

Byte #1 -- I^2C Slave Address.

Byte #2 – LSB Address

Byte #3 – MSB Address

Byte #4 – Attribute Table Entry to use for the following characters.

Byte #5 – First display character, SL parameter, RE or WE control code.

Byte #6 – Second display character, SL parameter, RE or WE control code.

Byte #7 – Third display character, SL parameter, RE or WE control code.

.

.

Byte #n – Last display character in this color sequence, SL parameter, RE or WE control code to use the associated Attribute Table Entry.

The Attribute Table Entry (Byte #4, of the above) is automatically associated with each subsequent display character or SL code written. The following is a graphical example of how the Display Page RAM associates to the actual On-Screen Display Window #1.

EXAMPLE #1:

A 3X3 character matrix of yellow characters on a black background is to be displayed on the screen of all the same color, using 2-color character codes:

Actual On-Screen Display of Window #1:

Notes:

- Every row must begin with an SL value. Display Page RAM memory location 8000h will always be associated with the SL of row 0 of Display Window #1.
- Every row except the last row of a Display Window must end with an RE character. The character immediately after an RE character is always the SL value for the next row.
- The last row in a Display Window must be a WE character. The WE character must NOT be preceded by an RE character.
- The entire Display Window may be written in a single I^2C write sequence because the Attribute Table entry (ie the color palette) does not change for the entire Display Window.
- The Attribute Table Entry that associated with RE and WE characters are "don't cares". So in general it is most efficient just to allow them to be the same value as the Attribute Table Entry associated with the previous display character.
- The colors of the characters and background can be stored in a single location in the 2-color attribute table, in location ATT1.

The contents of the display RAM are programmed as follows:

Address	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh
Attribute	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1
Contents	SL'0'	C'A'	C'B'	C'C'	RE	SL'0'	C'D'	C'E'	C'F'	RE	SL'0'	C'G'	C'H'	C'I'	WE

KEY: Att_ - Attribute Table Entry. The entire Window in this example uses the same Attribute Table Entry.

SL'**n**' - Skipped Line Parameter '**n**'.

RE - Row-end Character.

WE - Window-end Character.

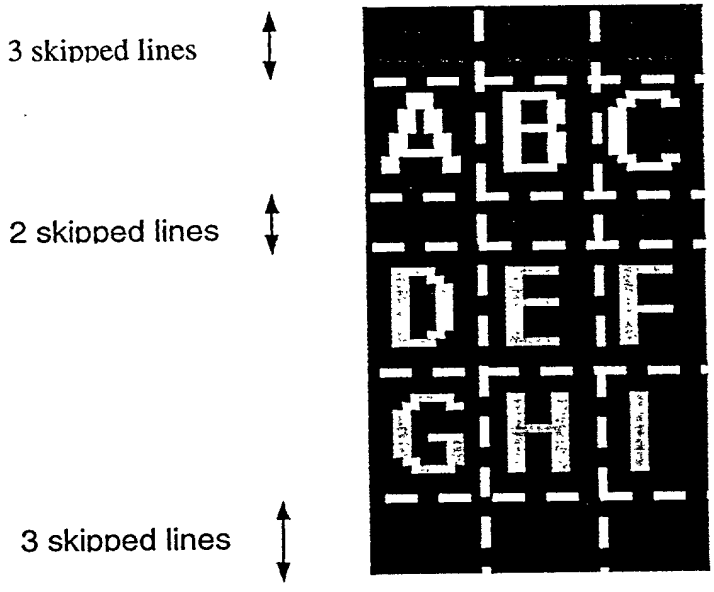
C'**A**' - Display Character value of character '**A**'.

In this example, SL is zero, as zero skipped lines are required.

EXAMPLE #2:

A 3X3 character matrix of characters on a black background is to be displayed on the screen, using 2-color character codes. 3 skipped lines are required above and below the characters, and between the first and second displayed character rows:

Actual On Screen Display of Window Example #2:



Notes:

- Every row must begin with an SL value. Display Page RAM memory location 8000h will always be associated with the SL of row 0 of Display Window #1.
- Every row except the last row of a Display Window must end with an RE character. The character immediately after an RE character is always the SL value for the next row.
- The last row in a Display Window must be a WE character. The WE character must NOT be preceded by an RE character.
- In order to create the skipped lines at the top of the page, a row of three 'blank' transparent characters must be used above the displayed area. In this example, these are defined by the 2-color attribute table entry ATT1. Bit 4 of Frame Control Register 1 must be set to indicate that the black color is to be translated as transparent (see section ' Control Register Definitions)
- The top row of characters are yellow on black; in this example, these are defined by the 2-color attribute table entry ATT9
- The second and third row of characters are blue on black; in this example, these are defined by the 2-color attribute table entry ATT10

The contents of the display RAM are as follows:

Address	0h	1h	2h	3h	4h	05h	06h	07h	08h	09h	0Ah
Attribute	Att9	Att1	Att1	Att1	Att9	Att9	Att9	Att9	Att9	Att10	Att10
Contents	SL'3'	C'_'	C'_'	C'_'	RE	SL'2'	C'A'	C'B'	C'C'	RE	SL'0'

Address	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h
Attribute	Att10	Att10	Att10	Att10	Att10	Att10	Att10	Att10	Att10
Contents	C'D'	C'E'	C'F'	RE	SL'3'	C'G'	C'H'	C'I'	WE

KEY: Att_ - Attribute Table Entry. The entire Window in this example uses the same Attribute Table Entry.

SL'**n**' - Skipped Line Parameter '**n**'.

RE - Row-end Character.

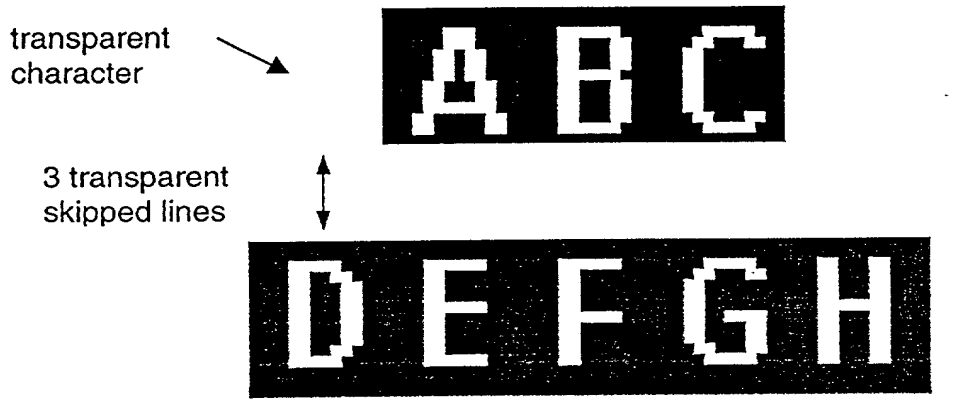
WE - Window-end Character.

C'_' - Display Character value of a blank character

EXAMPLE #3:

Two different length rows of characters a black background are to be displayed on the screen, using 2-color character codes. 3 transparent skipped lines are required between the character rows:

Actual On Screen Display of Window Example #3:



Notes:

- In order to centralize the three characters above the five characters on the row below, a 'transparent' blank character has been used as the first character on the row.
- In order to create the transparent skipped lines between the two character rows, a row of no characters has been used, resulting in a RE, SL, RE, SL control code sequence.
- In this example, the transparent lines and characters are defined by the 2-color attribute table entry ATT1. Bit 4 of Frame Control Register 1 must be set to indicate that the black color is to be translated as transparent (see section ' Control Register Definitions)
- The top row of characters are yellow on black; in this example, these are defined by the 2-color attribute table entry ATT9
- The second row of characters are blue on black; in this example, these are defined by the 2-color attribute table entry ATT10

The contents of the display RAM are as follows:

Address	0h	1h	06h	07h	08h	09h	0Ah	09h	0Ah
Attribute	Att1	Att1	Att9	Att9	Att9	Att9	Att1	Att10	Att10
Contents	SL'0'	C'_'	C'A'	C'B'	C'C'	RE	SL'3'	RE	SL'0'

Address	0Bh	0Ch	0Dh	10h	11h	13h
Attribute	Att10	Att10	Att10	Att10	Att10	Att10
Contents	C'D'	C'E'	C'F'	C'G'	C'H'	WE

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3.6 CONTROL REGISTER DEFINITIONS

Frame Control Register 1 (I^2C address 8400h).

REGISTER NAME: FRMCTRL1

Bit 7 Bit 0

RSV	RSV	RSV	TE	CDPR	D2E	D1E	OsE

Bit 0: On-Screen Display Enable. The On-Screen Display will be disabled when this bit is a zero. When this bit is a one the On-Screen Display will be enabled and Display Window 1 will be enabled if Bit 1 of this register is a one; likewise Display Window 2 will be enabled if Bit 2 of this register is a one.

Bit 1: Display Window 1 Enable. When Bit 0 of this register and this bit are both ones, Display Window 1 is enabled. If either bit is a zero, then Display Window 1 will be disabled.

Bit 2: Display Window 2 Enable. When Bit 0 of this register and this bit are both ones, Display Window 2 is enabled. If either bit is a zero, then Display Window 2 will be disabled.

Bit 3: Clear Display Page RAM. Writing a one to this bit will result in setting all of the Display Page RAM values to zero. This bit is automatically cleared after the operation is complete.

Bit 4: Transparent Disable. When this bit is a zero, a palette color of black (ie color palette look-up table value of '000 000 000') in Color 1 of the first 8 palette look-up table address locations (ie ATT = 0h-7h) will be translated as transparent. When this bit is a one, the color will be translated as black.

Bits 7-4: RESERVED.

Frame Control Register 2 (I^2C address 8401h).

REGISTER NAME: FRMCTRL2

Bit 7 Bit 0

PL2	PL1	PL0	BP4	BP3	BP2	BP1	BP0

Bit 4-0: Blinking Period. These five bits set the blinking period of the blinking feature., which is determined by multiplying the value of these bits by 8, and then multiplying the result by the vertical field rate.

Bits 7-5: Pixels per Line. These three bits determine the number of Pixels per line.

Bits 5-3	Description	Max Fh
000b	512 pixels per line	125kHz
001b	576 pixels per line	125kHz
010b	640 pixels per line	125kHz
011b	704 pixels per line	125kHz
100b	768 pixels per line	125kHz
101b	832 pixels per line	115kHz
110b	896 pixels per line	107kHz
111b	960 pixels per line	100kHz

Bits 7-6: RESERVED.

Note: the pixels per line must be set in conjunction with the PLL lock range as per the figure below. Note that the maximum horizontal frequency of the three highest resolutions is limited.

DS007204-45 DS007204-46

PLL RANGES

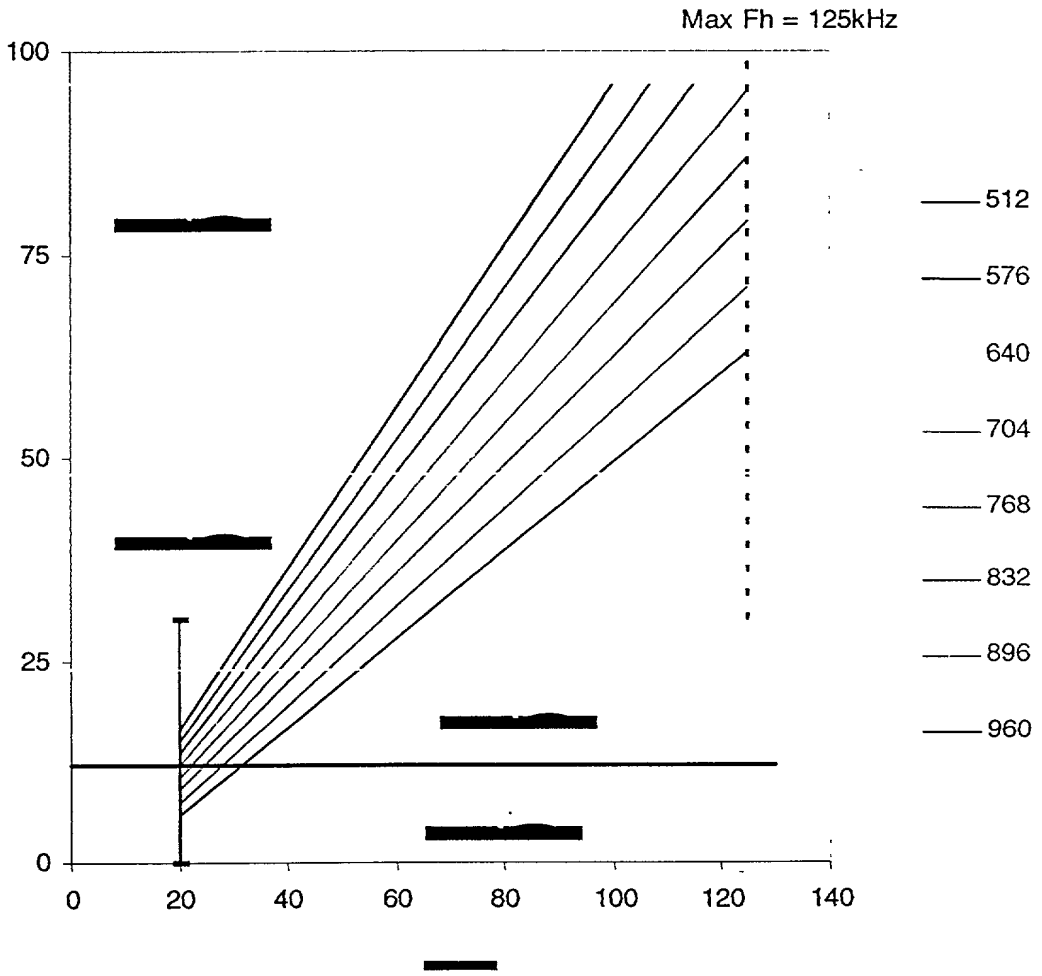

Figure 24 PLL LOCK RANGES

Character Font Access Control Register (I^2C address 8402h).

REGISTER NAME: CHARFONTACC

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	C/A	Bit

Bit 0: Four-color pixel data value Bit indicator. This bit indicates if Bit 0 (when a zero) or Bit 1 (when a one) of the four-color pixel data value is being accessed via I2C addresses 3000h – 3FFFh.

Bit 1: Character/Attribute Code Indicator. This bit controls what value is read via I2C reads of the Display Page RAM (address range 8000h-81FFh). When this bit is a 0, such reads will return the character code. When this bit is a 1, the attribute code will be returned.

Bits 7-2: RESERVED.

Vertical Blank Duration Control Register (I^2C address 8403h).

REGISTER NAME: VBLANKDUR

Bit 7 Bit 0

RSV	VB6	VB5	VB4	VB3	VB2	VB1	VB0

Bits 6-0: Vertical Blank Duration. These seven bits set the duration of the VBLANK signal in numbers of horizontal scan lines.

Bit 7: RESERVED.

OSD Character Height Control Register (I^2C address 8404h).

REGISTER NAME: CHARHTCTRL

Bit 7 Bit 0

CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7-0: Character Height: this register sets the character height according to the constant character height mechanism described in section Constant Character Height Mechanism. The value programmed in the register is equal to the approximate number of OSD height compensated lines required on the screen divided by 4. The value is only approximate, due to the approximation used in scaling the characters.

Example: If approximately 384 OSD lines are required on the screen (regardless of the number of image lines) then the Character Height Control Register is programmed with the value of 81.

Button Box Highlight Color Register (EF1) (I^2C address 8405h-8406h).

REGISTER NAME: BBHLCTRLB1 (8406h) BBHLCTRLB0 (8405h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0

Bits 8-0: Button Box highlight color. This register indicates the value of Enhanced Feature (button box highlight) register EF1.

Bits 15-9: RESERVED.

Button Box Lowlight Color Register (EF2) (I^2C address 8407h-8408h).

REGISTER NAME: BBLLCTRLB1 (8408h) BBLLCTRLB0 (8407h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0

Bits 8-0: Button Box lowlight color. This register indicates the value of Enhanced Feature (button box lowlight) register EF2.

Bits 15-9: RESERVED.

Heavy Button Box Lowlight / Shadow /Shading Color Register (EF3) (I^2C address 8409h-840Ah).

REGISTER NAME: CHSDWCTRLB1 (840Ah) CHSDWCTRLB0 (8409h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0

Bits 8-0: Heavy Button Box lowlight /shadow color. This register indicates the value of Enhanced Feature (heavy button box lowlight or shadow/shading) register EF3.

Bits 15-9: RESERVED.

ROM Signature Control Register (I^2C address 840Dh).

REGISTER NAME: ROMSIGCTRL

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	CRS

Bit 0: Calculate ROM Signature. Setting this bit causes the entire ROM to be read, sequentially, and a 16 bit CRC calculated over its contents. The residual value from this calculation is placed in the ROM Signature Data register. This bit automatically clears itself when the calculation has been completed.

Bits 7-1: RESERVED.

ROM Signature Data Register (I^2C address 840Eh-840Fh).

REGISTER NAME: ROMSIGDATAB1 (840Fh) ROMSIGDATAB0 (840Eh)

Bit 15 Bit 8 Bit 7 Bit 0

CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

Bits 15-0: ROM Signature Data. This register indicates the residual value from the

CRC calculation. Devices containing ROMs with different programming will give different signatures. Devices with the same ROM programming will give the same signature.

Display Window 1 Horizontal Pixel Start Location Register (I^2C address 8410h).

REGISTER NAME: HSTRT1 (8410h)

Bit 7 Bit 0

1H7	1H6	1H5	1H4	1H3	1H2	1H1	1H0

Bit 7-0: Display Window 1 Horizontal Pixel Start Location. These seven bits determine the starting horizontal pixel location, which is determined by multiplying the value of these bits by 4 and adding 30pixels. Due to pipeline delays, the first usable location for the OSD window is approx 42 pixels to the right of the horizontal flyback pulse. For this reason, the display start location must be programmed with a number larger than 2, otherwise improper operation may occur.

Display Window 1 Vertical Pixel Start Location Register (I^2C address 8411h).

REGISTER NAME: VSTRT1 (8411h)

Bit 7 Bit 0

1V7	1V6	1V5	1V4	1V3	1V2	1V1	1V0

Bit 7-0: Display Window 1 Vertical Pixel Start Location. These eight bits determine the starting vertical pixel location in constant height character lines, which is determined by multiplying the value of these bits by 2. (Note, each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the character cell size – see section Constant Character Height Mechanism).

Display Window 1 Column Width Control Register (I^2C address 8414h-8417h).

REGISTER NAME: COLWIDTH1B3 (8417h) COLWIDTH1B2 (8416h) COLWIDTH1B1 (8415h) COLWIDTH1B0 (8414h)

Bit 31 Bit 16

COL31	COL30	COL29	COL28	COL27	COL26	COL25	COL24	COL23	COL22	COL21	COL20	COL19	COL18	CRC17	COL16

Bit 15 Bit 0

COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL 8	COL 7	COL 6	COL 5	COL 4	COL 3	COL 2	COL 1	COL 0

Bits 31-0: Display Window 1 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31-0 of Display Window 1, respectively. A value of zero indicates the column will have normal width (12 pixels). A value of one indicates the

column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations.

The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

Display Window 2 Horizontal Pixel Start Location Register (I^2C address 8418h).

REGISTER NAME: HSTRT2 (8418h)

Bit 7 Bit 0

2H7	2H6	2H5	2H4	2H3	2H2	2H1	2H0

Bit 7-0: Display Window 2 Horizontal Pixel Start Location. These seven bits determine the starting horizontal pixel location, which is determined by multiplying the value of these bits by 4.

Display Window 2 Vertical Pixel Start Location Register (I^2C address 8419h).

REGISTER NAME: VSTRT2 (8419h)

Bit 7 Bit 0

2V7	2V6	2V5	2V4	2V3	2V2	2V1	2V0

Bit 7-0: Display Window 2 Vertical Pixel Start Location. These eight bits determine the starting vertical pixel location in constant height character lines, which is determined by multiplying the value of these bits by 2. (Note, each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the character cell size – see section Constant Character Height Mechanism).

Display Window 2 Starting Address in the Display Page RAM (I^2C address 841Ah-841Bh).

REGISTER NAME: W2STRTADRH (841Bh) W2STRTADRL (841Ah)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	2ad8	2ad7	2ad6	2ad5	2ad4	2ad3	2ad2	2ad1	2ad0

Bits 8-0: Display Window 2's Starting Address in the Display Page RAM. This register determines the starting address of Display Window 2 in the Display Page RAM. This first address location will always contain the SL code for the first row of Display Window 2.

Bits 7-5: RESERVED.

Display Window 2 Column Width Control Register (I^2C address 841Ch-841Fh).

REGISTER NAME: COLWIDTH2B3 (841Fh) COLWIDTH2B2 (841Eh) COLWIDTH2B1 (841Dh) COLWIDTH2B0 (841Ch)

Bit 31 Bit 24 Bit 23 Bit 16

COL31	COL30	COL29	COL28	COL27	COL26	COL25	COL24	COL23	COL22	COL21	COL20	COL19	COL18	CRC17	COL16

Bit 15 Bit 8 Bit 7 Bit 0

COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL 8	COL 7	COL 6	COL 5	COL 4	COL 3	COL 2	COL 1	COL 0

Bits 31-0: Display Window 2 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31-0 of Display Window 2, respectively. A value of zero indicates the column will have normal width (12 pixels). A value of one indicates the column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations.

The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

Built In Self Test Control Register (I^2C address 8420h).

REGISTER NAME: BISTCONTROL (8420h)

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	BFAIL	BEN

Bit 0: BIST Enable (BEN). Setting this bit causes the RAM built-in self test to be performed. This bit automatically clears itself when the test has completed.

Bit 1: BIST Fail (BFAIL). This bit indicates the results of the RAM built-in self test. After completion of the test, a 1 in this bit indicates a failure, and a 0 indicates success.

Bit 7-2: Reserved

Built In Self Test Address Register (I^2C address 8421-8422h).

REGISTER NAME: BISTADDR1 (8422h) BISTADDR0 (8421h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

Bits 8-0: Address (ADDR). These bits indicate address of the first failing location

Bit 15-9: Reserved

RAM BIST Compare Data Register (8423-8424)

REGISTER NAME: BISTCOMPARE1 (8424h) BISTCOMPARE0 (8423h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	CD11	CD10	CD9	CD 8	CD 7	CD 6	CD 5	CD 4	CD 3	CD 2	CD 1	CD0

Bits 11-0: COMPARE DATA. These bits indicate the data that was expected to be read from the first failing address.

RAM BIST Read Data Register (8425-8426)

REGISTER NAME: BISTREAD1 (8426h) BISTREAD0 (8425h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RD11	RD10	RD9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD0

Bits 11-0: READ DATA. These bits indicate the data that was actually read from the first failing address.

3.6.1 PRE-AMP INTERFACE REGISTERS

Red Channel Gain Control Register (I^2C address 8430h).

REGISTER NAME: RGAINCTRL (8430h)

Bit 7 Bit 0

RSV	RG6	RG5	RG4	RG3	RG2	RG1	RG0

Bits 6-0: Red Channel Gain Control. These seven bits determine the gain for the Red Channel.
Bit 7: RESERVED.

Blue Channel Gain Control Register (I^2C address 8431h).

REGISTER NAME: BGAINCTRL (8431h)

Bit 7 Bit 0

RSV	BG6	BG5	BG4	BG3	BG2	BG1	BG0

Bits 6-0: Blue Channel Gain Control. These seven bits determine the gain for the Blue Channel.

Bit 7: RESERVED.

Green Channel Gain Control Register (I^2C address 8432h).

REGISTER NAME: GGAINCTRL (8432h)

Bit 7 Bit 0

RSV	GG6	GG5	GG4	GG3	GG2	GG1	GG0

Bits 6-0: Green Channel Gain Control. These seven bits determine the gain for the Green Channel.

Bit 7: RESERVED.

Contrast Control Register (I^2C address 8433h).

REGISTER NAME: CONTRCTRL (8433h)

Bit 7 Bit 0

RSV	RSV	CG5	CG4	CG3	CG2	CG1	CG0

Bits 5-0: Contrast Gain Control. These six bits determine the overall gain of all three channels.

Bits 7-6: RESERVED.

Red Bias Clamp Pulse Amplitude Control Register (I^2C address 8434h).

REGISTER NAME: RBIASCTRL (8434h)

Bit 7 Bit 0

RSV	RSV	RC5	RC4	RC3	RC2	RC1	RC0

Bits 5-0: Red Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

Blue Bias Clamp Pulse Amplitude Control Register (I^2C address 8435h).

REGISTER NAME: BBIASCTRL (8435h)

Bit 7 Bit 0

RSV	RSV	BC5	BC4	BC3	BC2	BC1	BC0

Bits 5-0: Blue Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

AC2DC

Green Bias Clamp Pulse Amplitude Control Register (I^2C address 8436h).

REGISTER NAME: GBIASCTRL (8436h)

Bit 7 Bit 0

RSV	RSV	GC5	GC4	GC3	GC2	GC1	GC0

Bits 5-0: Green Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

Brightness Amplitude Control Register (I^2C address 8437h).

REGISTER NAME: BRIGHTCTRL (8437h)

Bit 7 Bit 0

RSV	RSV	BA5	BA4	BA3	BA2	BA1	BA0

Bits 5-0: Brightness Amplitude Control. These six bits determine the amplitude of brightness for all three channels.

Bits 7-6: RESERVED.

DC Offset and OSD Contrast Control Register (I^2C address 8438h).

REGISTER NAME: DCOFFSET (8438h)

Bit 7 Bit 0

BP2	BP1	BP0	OSD C1	OSD C0	DC2	DC1	DC0

Bits 2-0: DC Offset Control. These three bits determine the active video DC offset to all three channels.

Bits 4-3: OSD Contrast. These two bits determine the OSD contrast.

Bits 7-5: Blanking pedestal. These three bits determine the blanking pedestal offset for all three channels.

Global Video Control Register (I^2C address 8439h).

REGISTER NAME: GLOBALCTRL (8439h)

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	PS	BV

Bit 0: Blank Video. When this bit is a one, blank the video output. When this bit is a zero allow normal video out.

Bit 1: Power Save. When this bit is a one, shut down the analog circuits to support

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sleep mode. When this bit is a zero enable the analog circuits for normal operation.

Bits 7-2: RESERVED.

PLL Frequency Range Control Register (I^2C address 843Eh).

REGISTER NAME: PLLFREQRNG (843Eh)

Bit 7 Bit 0

RSV	RSV	IVIG1	IVIG0	IVS1	IVS0	PFR1	PFR0

Bit 1-0: PLL Frequency Range Control. These bits assist the PLL in locking to the desired pixel frequency. They are set based upon the desired pixel frequency range as follows:

00b if desired OSD pixel frequency is between 6MHz and 12MHz

01b if desired OSD pixel frequency is between 12MHz and 24MHz

10b if desired OSD pixel frequency is between 24MHz and 48MHz

11b if desired OSD pixel frequency is between 48MHz and 96MHz

Bits 3-2: IVISTAT. These bits control the minimum current of the V to I block of the PLL. The normal value of these bits is 01. These will not normally be altered by the user.

Bits 5-4: IVIGAIN. These bits control the gain of the V to I block of the PLL. The normal value of these bits is 01. These will not normally be altered by the user.

The PLL range shgould be set according to the table below:

PIXEL MODE	RANGE 0	RANGE 1	RANGE 2	RANGE 3
512	20-38	36-48	46-95	92-125
576	20-22	20-42	40-84	81-125
640	NA	20-39	37-76	73-125
704	NA	20-35	33-69	66-125
768	NA	20-32	30-64	61-125
832	NA	20-30	28-58	55-115
896	NA	20-28	26-54	52-107
960	NA	20-26	24-50	48-100

As IVIGAIN and IVISTAT are not normally changed by the user, the PLL Frequency Control Register should normally be written with the following values, depending upon the range of operation required:

RANGE 0	RANGE 1	RANGE 2	RANGE 3
14h	15h	16h	17h

Software Reset and Test Control Register (I^2C address 843Fh).

REGISTER NAME: SRTSTCTRL (843Fh)

Bit 7 Bit 0

PCT	AID	TEE	MUX1	MUX0	BCE	RSV	SRST

Bit 0: Software Reset. Setting this bit causes a software reset. All registers (except this one) are loaded with their default values. All operations currently in progress are aborted (except for I2C transactions). This bit automatically clears itself when the reset has been completed.

Bit 1: Reserved

Bit 2: Bypass Clock Enable. Setting this bit deselects the PLL as the source of the pixel clock, and selects the ABL input as the source of the pixel clock.

Bits 4-3: Multiplexed Output Select (MUX). Setting these bits selects which signal will be routed to the SCL output when test mode is enabled.

00 selects static LOW output
01 selects Pixel Clock from PLL
10 selects POWERGOOD signal from Power Quality Monitor
11 selects Horizontal rate feedback signal from PLL

Bit 5: Test Enable Enable. Setting this bit enables the CLAMP input to be used as a Test Enable input.

Bit 6: Auto Increment Disable. Setting this bit disables the automatic address increment feature of the I2C register access protocol. With this bit set, any I2C register may be continuously read or written without sending its address between register accesses.

Bit 7: Parallel Channel Test. Setting this bit causes the Red channel controls to apply to the Blue and Green channels, enabling ramp testing to be done in parallel on all 3 channels.

3.6.2 ATTRIBUTE TABLE AND ENHANCED FEATURES

Each display character and SL in the Display Page RAM will have a 4-bit Attribute Table entry associated with it. The user should note that two-color display characters and four-color display characters use two different Attribute Tables, effectively providing 16 attributes for two-color display characters and 16 attributes for four-color display characters.

For two-color characters the attribute contains the code for the 9-bit foreground color (Color 2), the code for the 9-bit background color (Color 1), and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, bordering, etc.).

For four-color characters the attribute contains the code for the 9-bit Color 1, the code for the 9-bit Color 2, the code for the 9-bit Color 3, the code for the 9-bit Color 4 and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, bordering, etc.).

3.6.3 TWO-COLOR ATTRIBUTE FORMAT

REGISTER NAME: ATT2C3n (8443h +(n*4)), ATT2C2n (8442h +(n*4)), where n = attribute code

Bit 31 Bit 24 Bit 23 Bit 16

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2R2	C2R1

REGISTER NAME: ATT2C1n (8441h +(n*4)), ATT2C0n (8440h +(n*4)), where n = attribute code

Bit 15 Bit 8 Bit 7 Bit 0

C2R0	C2B2	C2B1	C2B0	C2G2	C2G1	C2G0	C1R2	C1R1	C1R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0

Bits 8-0: Color 1. These nine bits indicate the value of the color to be displayed as color 1. This is considered to be the background color and is displayed when the corresponding pixel data bit is a zero.

Bits 17-9: Color 2. These nine bits indicate the value of the color to be displayed as color 2. This is considered to be the foreground color and is displayed when the corresponding pixel data bit is a one.

Bits 21-18: Enhanced Feature Bits. The enhanced features are determined as follows:

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Bits 21-18	Description
0000b	Normal (no enhanced features enabled).
0001b	Blinking.
0010b	Shadowing.
0011b	Bordering.
01XXb	RESERVED.
1000b	Raised Box.
1001b	Blinking and Raised Box.
1010b	Depressed Box.
1011b	Blinking and Depressed Box.
1100b	Heavy Raised Box.
1101b	Blinking and Heavy Raised Box.
1110b	Heavy Depressed Box.
1111b	Blinking and Heavy Depressed Box.

Bits 31-24: Reserved

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3.6.4 FOUR-COLOR ATTRIBUTE FORMAT

REGISTER NAME: ATT4C7n (8507h +(n*4)), ATT4C6n (8506h +(n*4)), where n = attribute code

Bit 63 Bit 56 Bit 55 Bit 48

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	C4R2	C4R1

REGISTER NAME: ATT4C5n (8505h +(n*4)), ATT4C4n (8504h +(n*4)), where n = attribute code

Bit 47 Bit 40 Bit 39 Bit 32

C4R0	C4B2	C4B1	C4B0	C4G2	C4G1	C4G0	C3R2	C3R1	C3R0	C3B2	C3B1	C3B0	C3G2	C3G1	C3G0

REGISTER NAME: ATT4C3n (8503h +(n*4)), ATT4C2n (8502h +(n*4)), where n = attribute code

Bit 31 Bit 24 Bit 23 Bit 16

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2R2	C2R1

REGISTER NAME: ATT4C1n (8501h +(n*4)), ATT4C0n (8500h +(n*4)), where n = attribute code

Bit 15 Bit 8 Bit 7 Bit 0

C2R0	C2B2	C2B1	C2B0	C2G2	C2G1	C2G0	C1R2	C1R1	C1R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0

Bits 8-0: Color 1. These nine bits indicate the value of the color to be displayed as color1. This is considered to be the background color and is displayed when the corresponding pixel data bit is 00b

Bits 17-9: Color 2. These nine bits indicate the value of the color to be displayed as color2. This is displayed when the corresponding pixel data bit is 01b

Bits 21-18: Enhanced Feature Bits. The enhanced features are determined as follows:

Bits 21-18	Description
0000b	Normal (no enhanced features enabled).
0001b	Blinking.
001Xb	RESERVED.
01XXb	RESERVED.
1000b	Raised Box.
1001b	Blinking and Raised Box.
1010b	Depressed Box.
1011b	Blinking and Depressed Box.
1100b	Heavy Raised Box.
1101b	Blinking and Heavy Raised Box.
1110b	Heavy Depressed Box.
1111b	Blinking and Heavy Depressed Box.

Bits 40-32: Color3. These nine bits indicate the value of the color to be displayed as color3. This is displayed when the corresponding pixel data bit is 10b.

Bits 49-41: Color4. These nine bits indicate the value of the color to be displayed as color4. This is displayed when the corresponding pixel data bit is 11b.

Bits 63-50: RESERVED.

3.6.5 ATTRIBUTE TABLES TO I^2C ADDRESS

	Two-color Attribute Table	Four-color Attribute Table
Attribute Value	I^2C Address	I^2C Address
0000b	8440h-8443h	8500h-8507h
0001b	8444h-8447h	8508h-850Fh
0010b	8448h-844Bh	8510h-8517h
0011b	844Ch-844Fh	8518h-851Fh
0100b	8450h-8453h	8520h-8527h
0101b	8454h-8457h	8528h-852Fh
0110b	8458h-845Bh	8530h-8537h
0111b	845Ch-845Fh	8538h-853Fh
1000b	8460h-8463h	8540h-8547h
1001b	8464h-8467h	8548h-854Fh
1010b	8468h-846Bh	8550h-8557h
1011b	846Ch-846Fh	8558h-855Fh
1100b	8470h-8473h	8560h-8567h
1101b	8474h-8477h	8568h-856Fh
1110b	8478h-847Bh	8570h-8577h
1111b	847Ch-847Fh	8578h-857Fh

3.6.6 BUTTON BOX FORMATION:

The value of the most significant Enhanced Feature Bit (EFB3) determines when to draw the left, right, bottom and top sides of a Box. EFB1 denotes whether a box is raised or depressed, and EFB2 denotes whether the box is normal or 'heavy'. For

normal boxes, the lowlight color is determined by the color code stored in the register EF2. For the heavy box feature, the lowlight is determined by color code stored in register EF3.

Boxes are created by a 'pixel override' system that overwrites character cell pixel information with either the highlight color (EF1) or low light shadow (EF2 or EF3) of the box. Only the top pixel line of the character and the right edge of the character can be overwritten by the pixel override system.

To form a complete box, the left hand edge of a box is created by overwriting the pixels in the right most column of the preceding character to one being enclosed by the box.

The bottom edge of a box is created by either

1. overwriting the pixels in the top line of the character below the character being enclosed by the box.

Or:

2. overwriting the pixels in the top line of the skipped lines below, in the case where skip lines are present below a boxed character.

Note: color selection EF2 or EF3 depends upon whether EFB2 is zero (EF2) or 1 (EF3).

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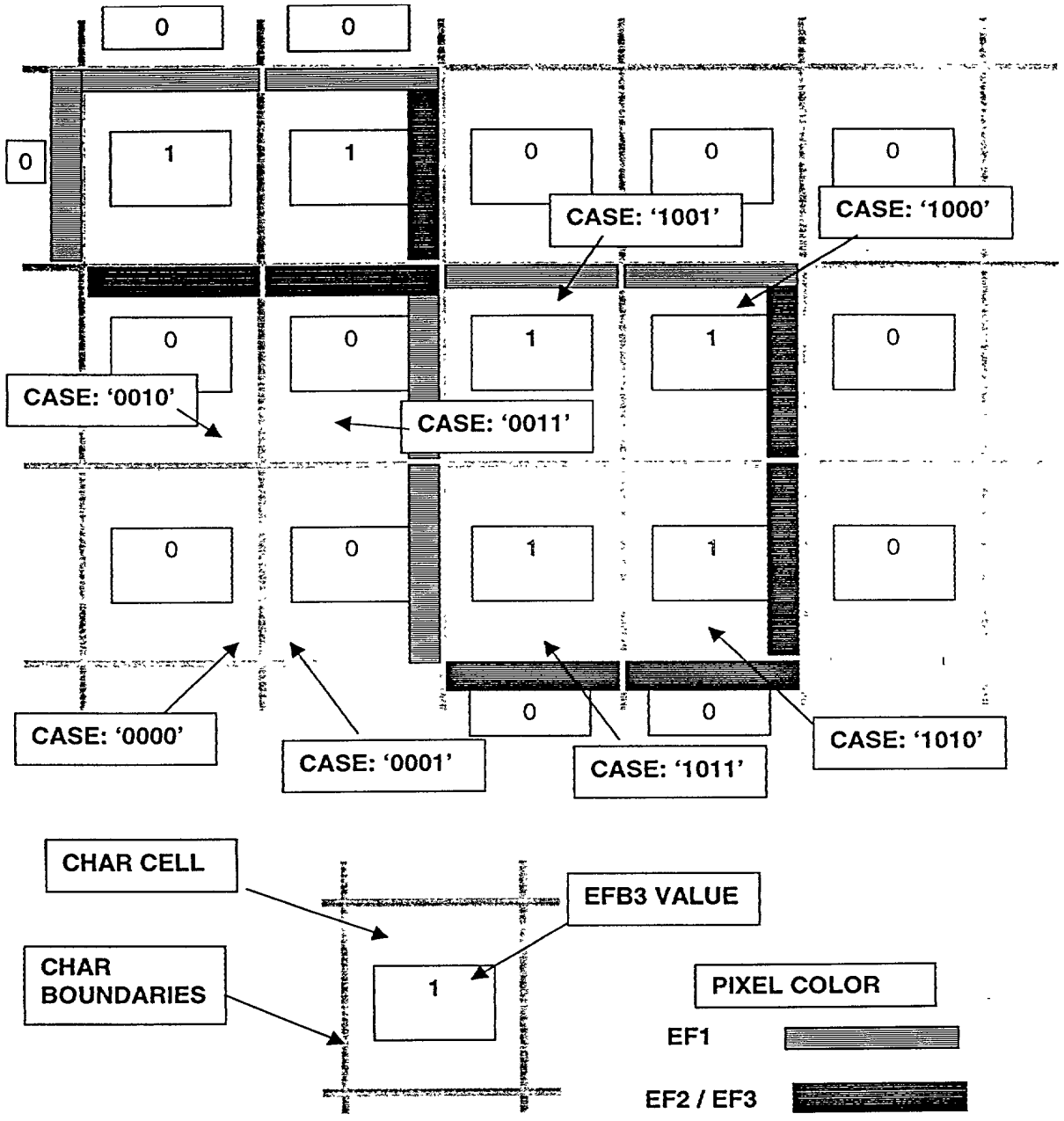

Figure 25 BUTTON BOX CONSTRUCTION (NO SKIP LINES)

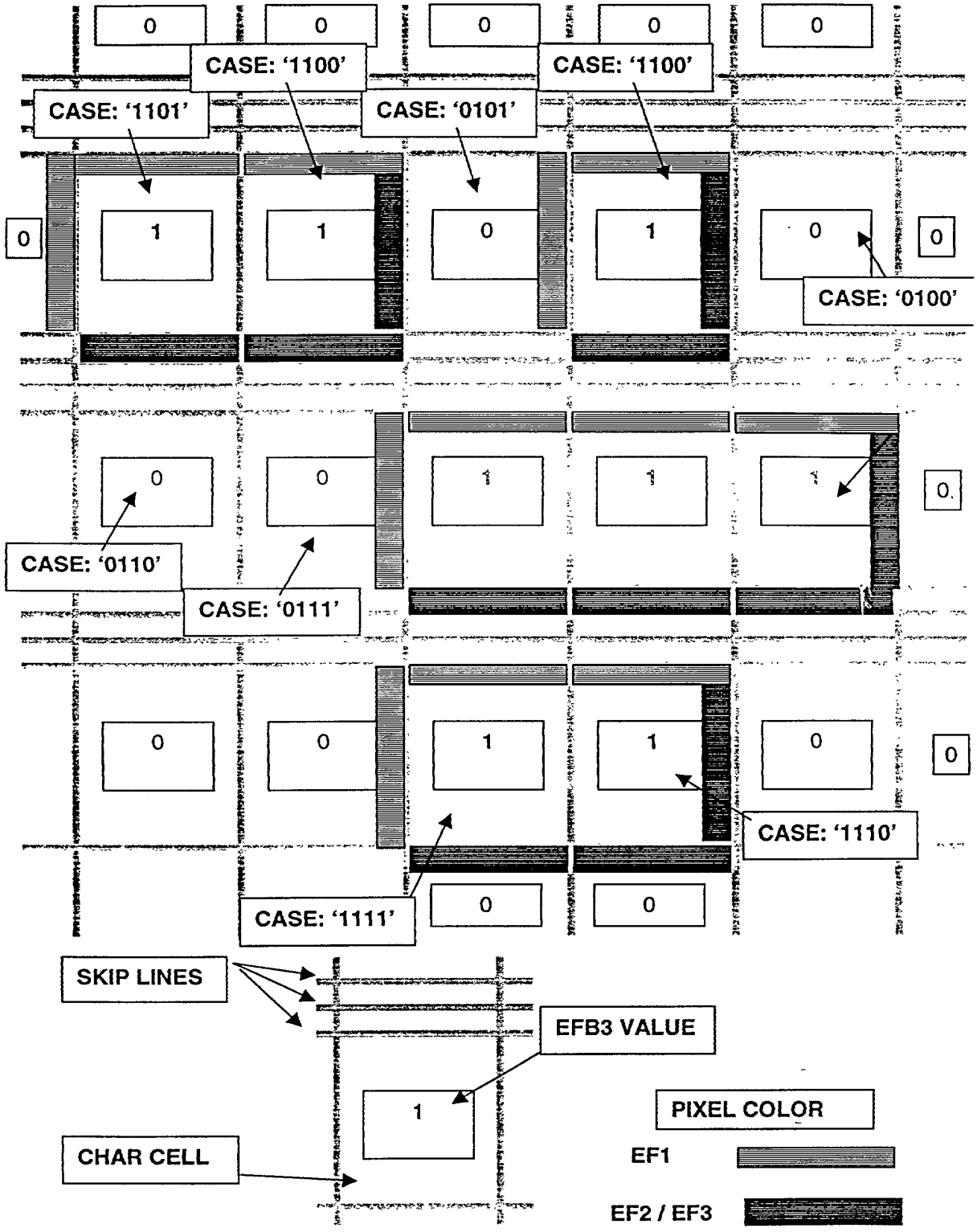

Figure 26 BUTTON BOX CONSTRUCTION (WITH SKIP LINES)

Some minor limitations result from the above box formation methodology:

- No box may use the left most display character in the Display Window, or it will have no left side of the Box. To create a box around the left most displayed character, a transparent 'blank' character must be used in the first character position. This character will not be visible on the screen, but allows the formation of the box.
- At least one skip line must be used beneath characters on the bottom row, if a box is required around any characters on this row in order to accommodate the bottom edge of the box.
- Skipped lines cannot be used within a box covering several rows
- Irregular shaped boxes, (ie other than rectangular), may have some missing edges.

3.6.7 OPERATION OF THE SHADOW FEATURE

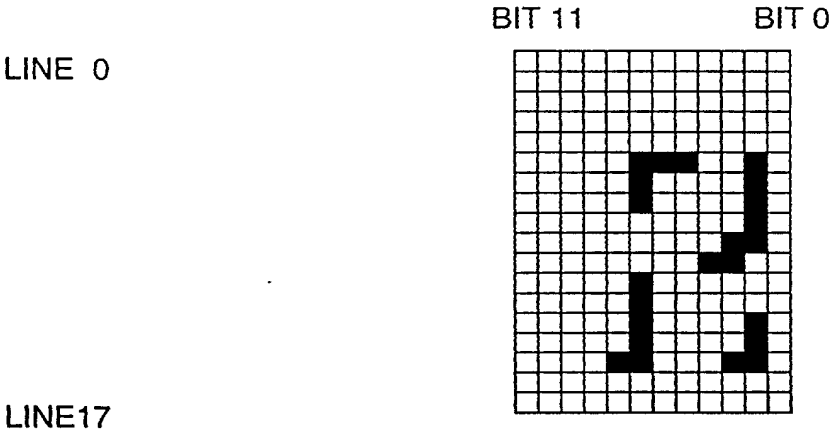

Figure 27 OPERATION OF THE SHADOW FEATURE

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3.6.8 OPERATION OF THE BORDERING FEATURE

Borders are created in a similar manner to the shadows, using the pixel override system to over write pixel data with a pixel color set by EF3.

Because the shadowing relies upon information about the pixels surrounding any given pixel, the bordering system may not operate correctly for pixels in line 0, line17, and column 0 and column 11.

3.7 CONSTANT CHARACTER HEIGHT MECHANISM

The CRT monitor scan circuits ensure that the height of the displayed image remains the constant, and so the physical height of a single displayed pixel row will decrease as the total number of vertical image lines increases. If the OSD character matrix has a fixed number of lines, C, (where C=18), then the character height will reduce as the number of scan lines increase, assuming a constant image height. To prevent this, the OSD generator repeats some of the lines in the OSD character in order to maintain a constant height.

The constant character height mechanism detects when interlace mode is being used and compensates to ensure the character height remains the same as for non-interlaced formats.

3.8 DISPLAY WINDOW1 TO DISPLAY WINDOW2 SPACING

There is no required vertical spacing between Display Window 1 and Display Window 2, but they should not overlap.

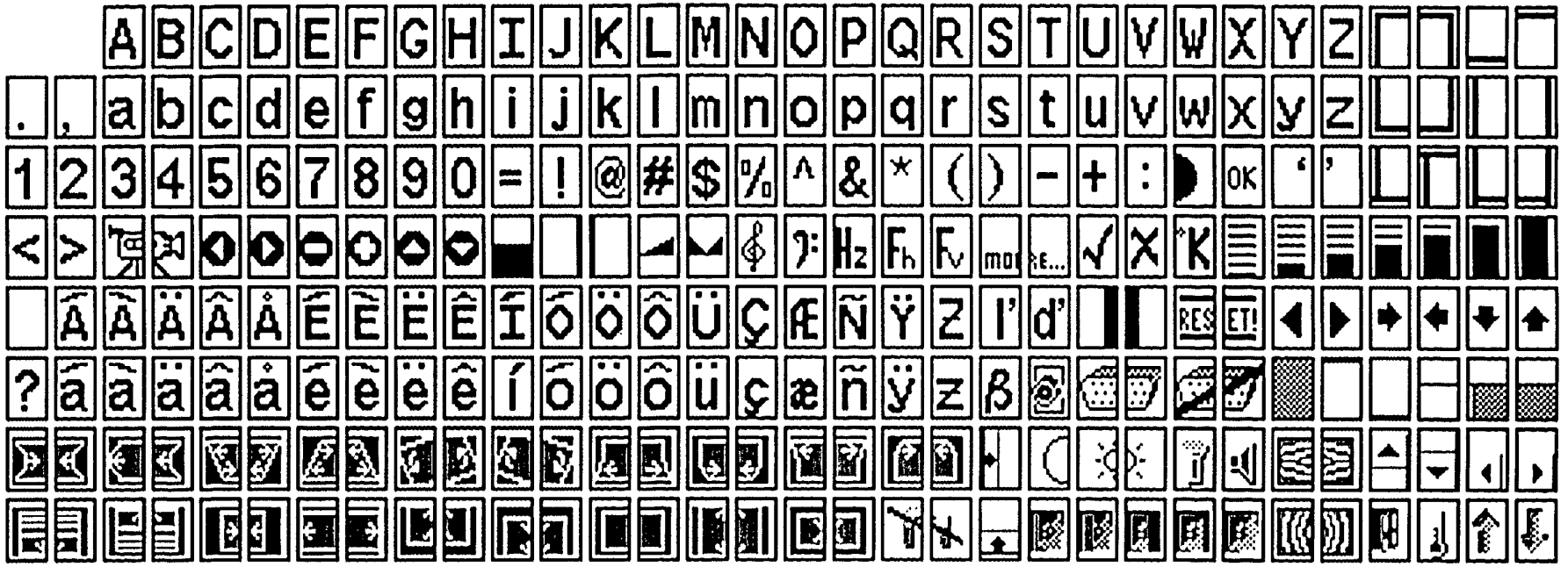
There must be a two character horizontal space between Display Window 1 and Display Window 2 for proper operation of both windows or undefined results may occur.

4 EVALUATION CHARACTER FONTS

The preliminary character font for evaluation of the LM1253 is shown in the figures below.

Also note that the first two character codes of the two color font (00h and 01h) are reserved for the Window End (WE) and Row End (RE) codes respectively.

00h



E0h

1Fh

FFh

Figure 28 EVALUATION CHARACTER FONT